EE Concierge Style Guide

PCB Layout and Component Creation

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Version

1.2

Table of Contents

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Introduction

Most style guides are horrible. Completely disconnected from actual design, written by some manager that hasn't actually done design in a decade, and filled with one person's preferences and "recommendations". This isn't those documents.

This represents the accumulated knowledge and best practices of 35,000+ electrical engineers, working on 100,000+ designs, while collaborating, sharing, and co-existing in the world's largest electrical engineering community, and its first professional cloud tool chain.

EE Concierge uses the Upverter toolset to service our requests because of its rapid, online, distributed and collaborative features. Upverter also supports exports to a variety of file formats allowing us to seamlessly deliver EE Concierge to the users of many different EDA toolsets. You will see Upverter mentioned throughout this document as a result. The EE Concierge team works very closely with the Upverter team, and we are partners in building and delivering this service.

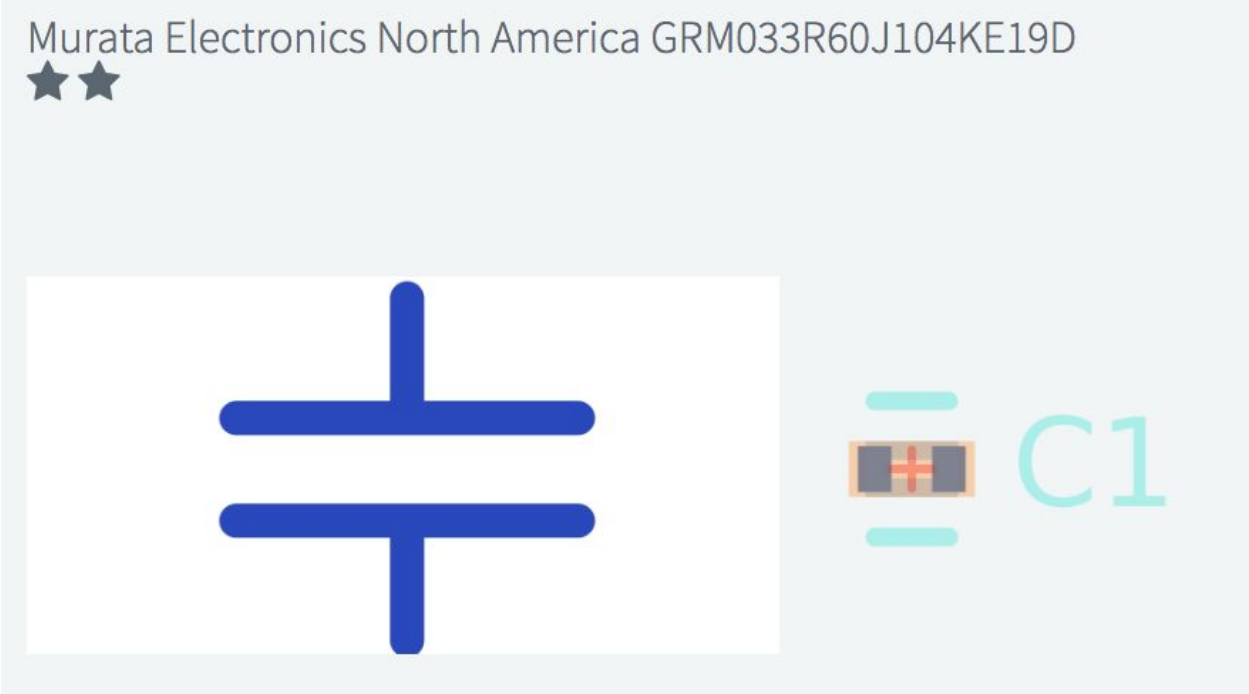
This guide started as a document originally written to help guide the dozen or so early EE Concierge Marketplace Contractors when we introduced the first ever parts concierge to the world. This was their guidebook for creating about 1,000 parts a week for thousands of engineers all over the world. It was critical that the parts they created be of the highest possible quality, yet at the same time be versatile enough to be used by any member of the EE Concierge community while still quick to create. It has grown profoundly since then, and will continue to evolve.

Much of what gets captured here will get implemented inside the Upverter tool chain. It's our hope that someday this guide is no longer necessary, having been completely subsumed into the Upverter tools and thus made obsolete. But for now, this guide is the absolute best source for how to design electronics both within Upverter, and without. This is a living document, we encourage you to add to it, voice your opinions, and help define the syntax of electrical engineering.

If you're an EE Concierge contractor, working on either component creation for the EE Concierge Parts Concierge, PCB layout (or any of our yet unreleased services) for the EE Concierge Design Services Group, or hardware manufacturing for the EE Concierge Fabrication Service you must read this guide. It should be your handbook and you must deliver work that passes the guidelines set down in this document.

If you're an Upverter user we also recommend following this guide. You will have the best possible experience using the Upverter toolset if you do.

Checklist: What a perfect part looks like



In order of priority, a perfect part contains all of the following:

1. **Complete and Detailed Part Attributes**
   All important part information is entered into Upverter and available to the end user.

2. **Pin Names Mapped to Pin Numbers**
   Every pin on the part is entered into Upverter exactly as they are in the datasheet.

3. **CAD Symbol**
   The symbol is the logical drawing of a part used in schematics. It includes 100% of the pins entered above, grouped in a useful and intelligent way. When a part has lots of pins, the pins, still grouped intelligently, are split between multiple symbols.

4. **CAD Footprint**
   The footprint is the physical drawing of the copper pads, paste, silkscreen, etc that a part gets soldered onto during manufacturing. It is exactly as specified in the datasheet, including pad sizes, thermal vias, etc. If not specified in the datasheet, the most aggressive (ie smallest pad sizes) generated IPC footprint is produced.

5. **3D STEP Model and Rotation and Translation Attributes (Optional)**
   Upverter parts can have 3D STEP models associated with them. This is an optional attribute, but when configured will point to a high definition STEP model of the exact package and dimensions from the datasheet.

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6. **Pin Directions and Signal Type**
   Pins are labelled with the proper direction / signal type (I/O, POWER, PASSIVE, etc) exactly as they are in the datasheet.

7. **Simulation Model (Optional)**
   Currently not available.

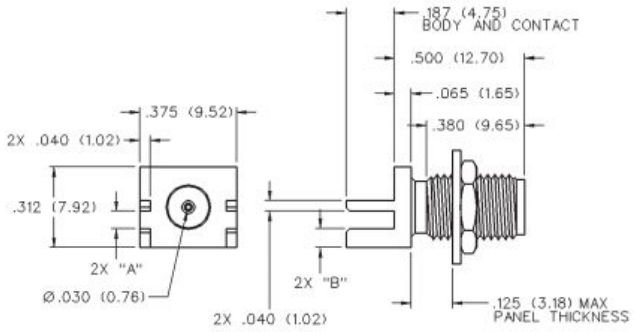
8. **Alternate or Replacement Parts (Optional)**
   Currently not available.

9. **Manufacturer Provided Reference Designs (Optional)**
   Currently not available.

Style Guide: Pins

This section walks through how to name and number pins when you're creating a part.

Number of Pins



These are the general rules of thumb to follow, when trying to decide how many pins a part has. For most parts this is extremely clear, where it becomes complicated is with connectors, mechanical features like mounting pins, and non-signal pins like ground pads. It's critical that you correctly identify the number the pins as having too many or too few pins will mark the entire part as incorrect.

What is a pin? A pin is a connection point in the schematic that also has at least one associated copper pad or plated hole. Every signal, power, and ground connection point is also a pin. The datasheet may not count up all of the ground pads, or housing connection points a part has, but you still need to make them into pins, because if a ground pad is just a blob of copper, and isn't

created as a pin then there is no way in the schematic to say that blob of copper needs to be connected to ground.

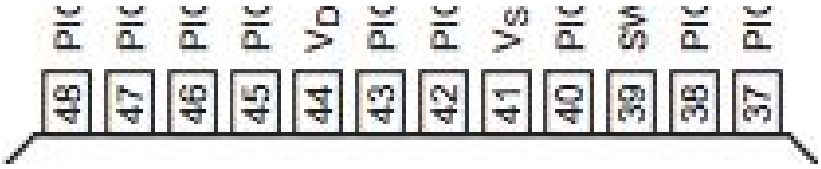
Any mounting point that needs a copper pad, even if does not require a connection, requires a pin.

1. If the datasheet does not explicitly name the mounting points and it does not specify that they need to be connected to GND then name the pins MNT_NUMBER (eg. MNT_1, MNT_2).
2. If the datasheet does not explicitly name the mounting points but it's specifies that they need to be connected to GND (such as a chassis ground) then group all of the mounting points together into a single pin and name it GND_C.
3. Alignment pins that use a non-plated hole do not get a pin.

Every single physical pin or pad that a part has should be created as a separate pin. In other words if a part has many physical ground pads, then the part you create should have just as many ground pins. The only exception to this is the housing: if a part has a grounded housing with multiple contact points, it should only be represented by a single pin which is then associated with each of the contact points.

In the picture above there is a board edge coax connector. It has 5 contact points: 3 on the top, and 2 on the bottom. 4 of these contact points are the housing (same net: ground), and 1 is the actual signal pin. This part should have 2 pins on the schematic, and 5 copper pads in the footprint, but 4 of these pads should be connected to the same pin.

Pin Numbers



These are the general rules of thumb to follow, when numbering the pins of a part. It's critical that you number the pins correctly as a single pin numbered incorrectly is enough to mark the entire part as incorrect.

For most 4+ pin count parts you will either see numeric pin numbers (example 1 through 8 for a standard 8 pin SOT part) or BGA style letter-number pairs (example A1 through D4 for a standard 16 pin BGA). You should number your pins in exactly the same way. Passives, 1, 2 & 3 pin parts, Transistors, Mosfets, etc are the exceptions to this.

1. Pins should be numbered exactly as they are in the datasheet. We expect you to number the pins inside Upverter identically to what the datasheet says.

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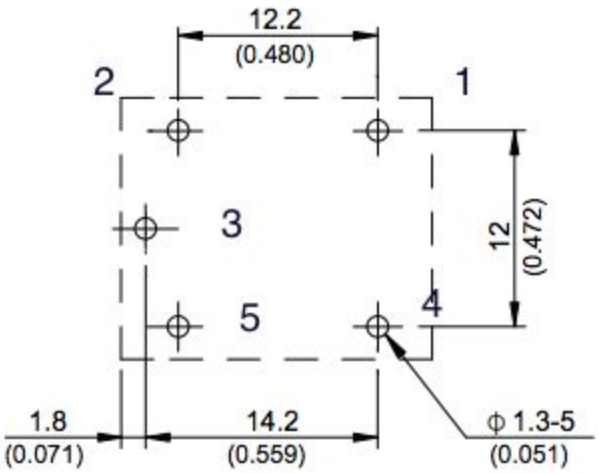
2. If there are no numbers in the datasheet, and the part is not a BGA, number the pins numerically starting with 1 and counting up.

3. If there are no numbers in the datasheet, and the part is a BGA, number the pins by giving each row a letter starting with A, and each column a number starting with 1. You should end up with a grid where each pin's number is the combination of the row letter and the column number.
4. All alphanumeric pin numbers should be uppercase (eg. TAB, A1).

5. If you've added pins that aren't listed in the datasheet (for example a ground pad) then they should be listed last in the pin list, with the next consecutive number. In the case of an 8 pin part with a ground pad, the pad would be number 9.

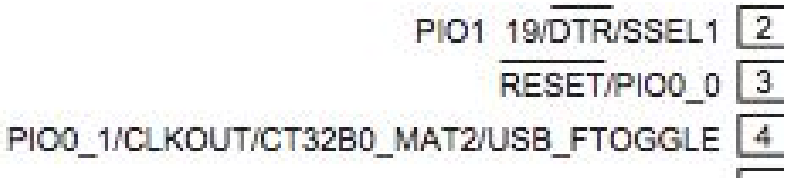
6. If the datasheet identifies pins as terminals or contacts (eg. Terminal 1, Terminal 2, Contact 1, Contact 2) number the pins 1,2,etc. Do **NOT** include the terminal or contact in the number (eg do **NOT** use TERMINAL_1) .

7. If there are no numbers in the datasheet, or the datasheet doesn't number all the pins, number the pins 1,2,3,etc based on the footprint in order from left to right and top to bottom.
    a. Example http://www.molex.com/pdm_docs/sd/5031821853_sd.pdf
    Pin Number and Names should be:
    1 = DATA2
    2 = CD/DAT3
    3 = CMD
    4 = vdd
    5 = CLK
    6 = Vss
    7 = DAT0
    8 = DAT1
    9 = MNT_1
    10 = MNT_2
    11 = SWITCH
    12 = MNT_3
    13 = DETECT
    14 = MNT_4
    15 = MNT_5
    b. If the recommended footprint is from "bottom view", flip the footprint left to right and follow the rule above. Example below is a bottom view recommended footprint:



8. For more pin numbering examples see the following document: https://docs.google.com/drawings/d/1hVWXDy9jkAUCF7nFn3dkZ4bPxTDdeTgLFqSpdktsrFM/edit?usp=sharing

Pin Names



These are the general rules of thumb to follow, when naming the pins of a part. It's critical that you name the pins correctly as a single pin named incorrectly is enough to mark the entire part as incorrect.

For larger components (50+ pins), use the .CSV import instead of manually typing in pin names/numbers, to avoid making a mistake. Try to copy the pin table from the datasheet into a Google spreadsheet. On a Mac, open the PDF in Preview and try selecting columns while holding the Option key. You'll probably discover other tricks too.

1. If possible you should use the manufacturer provided CSV file that contains the pin names. There is a feature inside upverter that allows you to upload this file and automatically creates pins for you.

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2. If a datasheet has a diagram and pin table, both show a pin number and pin name, then follow the diagram.
    a. This is most common in IC datasheets. The diagram has a simplified pin name and the table lists all of the additional functions. Use the simplified pin name because this will reduce the variation.

3. If a datasheet has a diagram and pin table, but only the table shows the pin number and pin name and the diagram is missing the pin number and/or pin names, then follow the table.
    a. This is common in a lot in transistor datasheets. The diagram will show a rough labelling of "this pin is the gate and this pin is the collector" but it won't have pin numbers. Oftentimes the datasheet will have a table in the mechanical section that specifically maps pin name to pin number. In these cases you want to use the table.

4. It may be faster and easier to copy and paste the pin names out of the datasheet, into a program like Excel and tidy them up, before either copying and pasting them into upverter - or saving the excel file as a CSV and uploading it to Upverter.

5. Do not change the order of the pin name. Write it down as it appears in the diagram / table (ex **PB0(I2C/MDIO/GPIO7)**).

6. Pins should be named exactly as they are in the datasheet. We expect you to name the pins inside Upverter identically to what the datasheet says.
    a. Do not abbreviate (shorten) names from the datasheet (ex. Do not change GROUND to GND or RESET to RST).
    b. Do not expand names from the datasheet (ex. Do not change GND to GROUND or RST to RESET)

7. Pin names should be capitalized exactly as they are in the datasheet.
    a. For example if the datasheet names a pin **Vin** then you should enter it as **Vin**, **not** as **VIN**.

8. If a pin is active low, it will usually be denoted with an overbar above the pin name, though occasionally with a # or ! character somewhere in the name or it may end with a n, N, _n, b, or B (for example: POWERGOODn, CSB). You need to start the pin name with **!** to mark the pin as active low in Upverter. You also need to exclude any extra # or ! or terminating n, _n characters from the name.
    a. For example POWERGOODn becomes !POWERGOOD, RST# becomes !RST, CSB becomes !CS, and Reset_n becomes !Reset.
    b. There is one exception to this rule. If the pin name is a series of functions such as gpmc_advn_ale which are separated in the pin name with _ and all the function (gpmc, advn, ale) are not active low. In such a case do not change the n (from advn) to !. In this example advn is active low but ale is active high. We allow this exception because if you used !, the system

would place an overbar over the whole pin name which is wrong. This case does not apply to cases that are separated by /. If the pin name was gpmc/advn/ale then the pin name should gpmc/!adv/ale.

9. There shall not be any spaces in pin names. Use underscores to separate multiple words or remove the spaces if they appear before or after / \ { } ( ) [ ].
    a. For example if a datasheet pin name is “Red Cathode” then the Upverter pin should be named Red_Cathode
    b. For example if a datasheet pin name is “PA5 (GPIO)” then the Upverter pin should be named PA5(GPIO)

10. Replace commas (,) and backslash \ with /
    a. For example if a datasheet pin name is “P0[3] (GPIO, OPAMP0-, EXTREF0)” then the Upverter pin should be named P0[3](GPIO/OPAMP0-/EXTREF0)
    b. For example if a datasheet pin name is “P0[3](GPIO\OPAMP0-\EXTREF0)” then the Upverter pin should be named P0[3](GPIO/OPAMP0-/EXTREF0)

11. For IC packages with an exposed pad (like thermal pad in the center), create an additional pin on the symbol that reflects what net the pad should be connected to. If the datasheet specifies a name for the exposed pad, call it **name_PAD**. If it’s a thermal pad that should be connected to ground, then call it **GND_PAD (VSS_PAD if datasheet uses VSS not GND)**. If it’s an output pin, call it **OUT_PAD**. If it’s a non-ground, non-output, not named in the datasheet exposed pad, call it **MNT_PAD**. **You must associate this extra pin with the corresponding pad on the layout.** Examples:
    a. If the exposed pad is connected internally to a specific signal, or is some kind of electrical signal then pin name = signal_PAD (eg. OUT_PAD, ANODE_PAD)
    b. If the exposed pad is supposed to be connected to GND/VSS then pin name = GND_PAD/VSS_PAD
        i. Make sure the datasheet specifies that pad needs to be connected to GND. There are times when the pad is internally connected to GND but it is NOT supposed to be connected to GND on the design (eg. temperature sensors). In this case follow point c below.
    c. If the exposed pad is not connected to GND or any signals and is purely for mechanical or thermal reasons then call it MNT_PAD. Even if the datasheet shows it as Thermal Pad or Exposed Pad, name the pin MNT_PAD.
    d. Do not treat DPAK / SOT component TABS as exposed pads.

12. If you’ve added chassis ground pins not explicitly named in the datasheet (for example a grounded mounting pin on a metal usb connector) then they should be named **GND_C**.
    a. Note: This is only done when the datasheet explicitly states that the mounting point needs to be connected to GND

13. Do not treat the tab pin of a DPAK or SOT component as an exposed pad with respect to naming. If the datasheet calls it DRAIN then use DRAIN as the pin name.

a. If the datasheet numbers the tab as TAB and not a number, then use TAB as the pin number in Upverter.
b. If the datasheet does not name the tab and does not identify that it needs to be connected to anything, call it MNT_PAD

14. If there are no names in the datasheet or are just labeled + and -, the part has only two pins, and it has polarity name pin 1 CATHODE and pin 2 ANODE.

15. If there are no names in the datasheet, and the part is a transistor name the pins EMITTER, BASE, and COLLECTOR.

16. If there are no names in the datasheet, and the part is a mosfet name the pins DRAIN, GATE, and SOURCE.

17. If there are no names in the datasheet, and the part has unconnected or unused pins name them NC (stands for no connect).

18. If there are no names in the datasheet, the part is an LED and the part has multiple colors, name them COLOR_CATHODE and COLOR_ANODE (eg. RED_CATHODE).

19. If there are no names in the datasheet, and the part has multiple different polarity, transistors, diodes, or mosfets, prepend them with numbers like this: NUMBER_BASE (eg. 1_BASE, 1_ANODE).

20. If the part is an ESD suppressor and there are no pin names in the datasheet, call the pins 1 and 2, **NOT** 1_Anode / 2_Anode. Below is an example of an ESD suppressor:

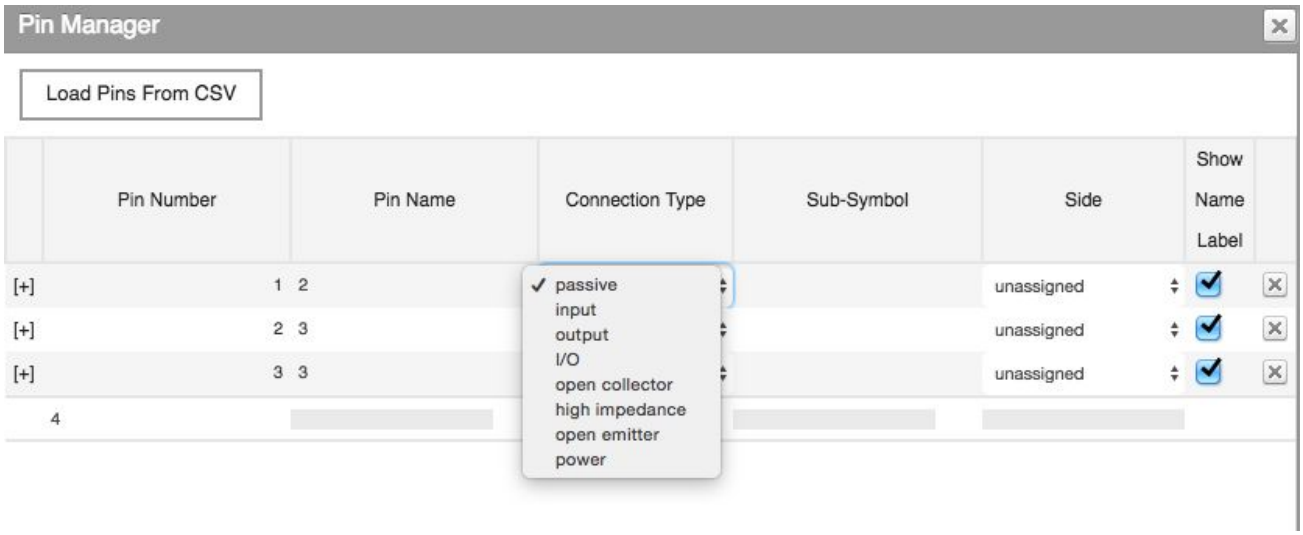
21. Do not use + and - signs to indicate polarity unless specifically directed by the datasheet (eg. GREEN+).

22. Do not use + and - signs to indicate power unless specifically directed by the datasheet (eg. +Vin).

23. If there are no names in the datasheet, and the part hasn't matched any of the other rules name the pins numerically starting with 1 and counting up.

24. For more pin naming examples see the following document: https://docs.google.com/drawings/d/1hVWXDy9jkAUCF7nFn3dkZ4bPxTDdeTgLFqSpdktsrFM/edit?usp=sharing

Pin Types

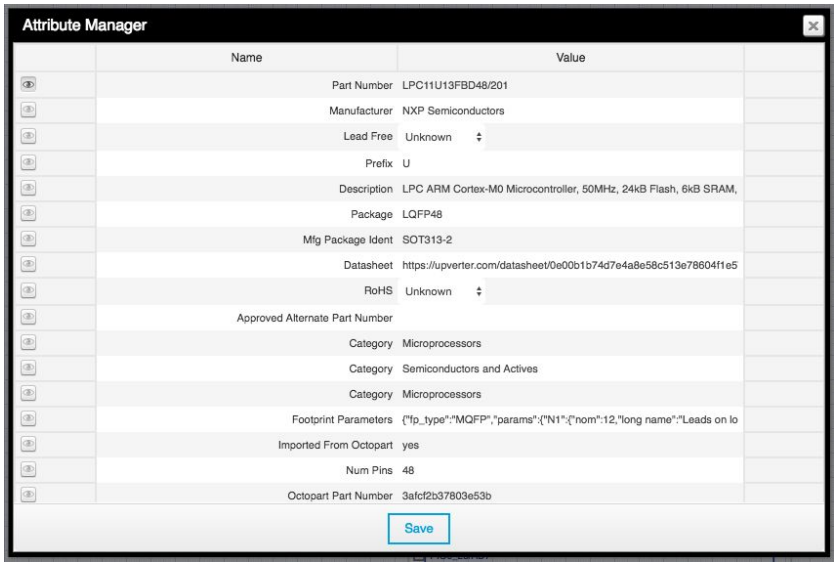


1. You should set the pin connection type (direction) on every pin as you create it. The options are as follows:
    a. Passive (default)
        i. Ex: resistor pins, capacitor pins, NC pins, IC configuration pins
    b. Input
        i. Ex: enable pins, reset pins, memory address pins, input clocks
    c. Output
        i. Ex. state flag pins, any signal named “output”
    d. I/O
        i. Ex: general purpose IO
    e. Open Collector
        i. Only use if datasheet specifically states open collector or open drain
    f. HiZ *(high impedance)*
        i. Ex: mosfet gate pin, OP AMP + and - input terminal pins
    g. Open Emitter
        i. Only use if datasheet specifically states open emitter
    h. Power
        i. Both positive / negative rails and GND

2. Be sure to set Power, Input, Output, and I/O whenever possible.

3. **IMPORTANT!!** If you can’t tell which type of pin it is and the datasheet does not provide details, just leaving it as “Passive”.

Style Guide: Attributes



This section covers how to setup attributes when you're creating a part.

Step by Step Walkthrough

1. Fill in all default attributes
    - ➢ **Part Number:**
        - This is the full, orderable part number that you'd find on a distributor website.
        - It includes the base part number as well a few characters after the part number representing things like thermal options, environmental options, package size, etc.
        - The only option that should be excluded from the part number is packaging type (cut tape, reel, etc) if it's an option.

    - ➢ **Manufacturer:**
        - Full name of the manufacturer that currently makes the part, like Texas Instruments instead of TI
        - When a part was historically made by one company, but is now made by a different company, or when a product line has been renamed, this attribute should be set to the newest manufacturer

    - ➢ **Lead Free:**
        - If a datasheet specifies the Lead-Free status then choose appropriately otherwise select unknown. You can also check digikey to confirm lead-free status.

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- **Prefix:**
  - Standard refdes prefixes:
    - ANT -- antenna
    - BT – battery
    - C – general capacitors
    - D – diodes (includes LEDs)
    - DS - display
    - ENC - Encoders
    - F - Fuse
    - FB - Ferrite bead
    - FC – fiducial
    - FL - filter
    - H – holes/vias (sometimes it makes sense to include specific components on the schematic to designate corresponding holes on the layout, like in DDR routing)
    - J – connectors (headers, video connectors, audio connectors, USB, etc.)
    - K -- relays
    - L – inductors and ferrites
    - LS - Loud speaker / buzzer
    - M - Motors
    - OP - op amp
    - Q – transistors
    - R – resistors
    - RG – power regulators (like LDOs). When in doubt, go with U.
    - RN – resistor networks
    - SW – switches
    - T – transformers
    - TP – test points
    - U – ICs
    - Y – crystals
    - For any not listed above follow the wikipedia page: https://en.wikipedia.org/wiki/Reference_designator

- **Description:**
  - Generally copy and paste the full title from the datasheet as it's usually a good description of the part. It's fine if this is long.

- **Package:**
  - It's difficult to develop naming conventions for packages, but some general guidelines are:
    - For standard packages, use the package name and pin count. (ex. SOT23-5, QFN32, QFN32-EP, FBGA584, TSSOP14, SOIC8, TO-92)

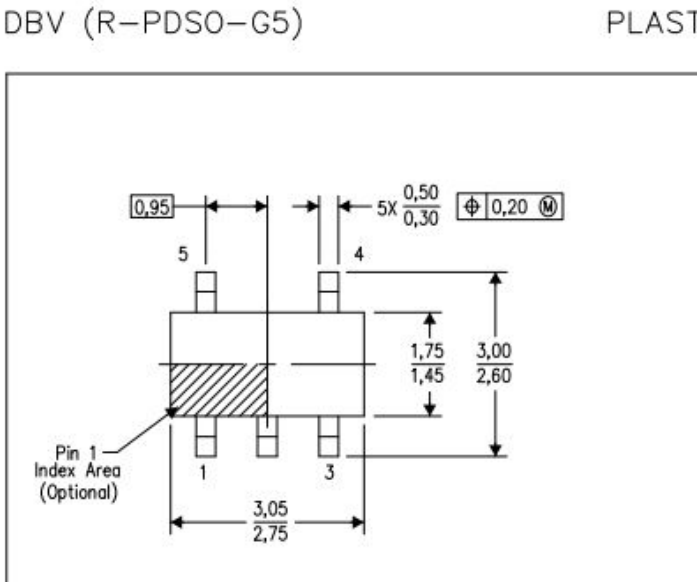
- For standard chip resistor and capacitor packages use the imperial package name and not the metric package name (ex. 0201, 0402, 0603, etc)
- For headers use HDR# where # is the number of pins (ex. HDR14 for a 14 pin header)
- For non-standard packages, like connectors, you'll have to make something up. Connectors start with CONN (CONN_USB, CONN_AUD_3MM5 for a 3.5mm audio jack, CONN_PTH_BNC for a through hole bnc connector, etc)
- Surface mount crystals/oscillators: e.g. 5.0 x 3.2 mm will be "SMT_XTAL_5MM0_3MM2"
- For axial and radial through-hole parts, simple name them AXIAL or RADIAL as appropriate (see picture below for the difference).

Axial- (top) and radial- (bottom) leaded electrolytic capacitors

- When in doubt, **ask for help!**

➢ **MFG Package Ident:**

- This is the identification number of a mechanical drawing.
- Not all datasheets will have this.
- The MFG package ident of the example below is DBV(R-PDSO-G5)



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- **Datasheet:**
  - This is the URL to the datasheet.
    - The best URLs point to the manufacturer's website directly. Worse, but better than nothing, are URLs that point to distributors or octopart.
    - Update this field to the latest datasheet.

- **RoHS:**
  - If a datasheet specifies the RoHS status then choose appropriately otherwise select unknown. You can also check digikey to confirm RoHS status.

- **Approved Alternate Part Number:**
  - Currently leave blank

- **Capacitance:**
  - Used only for capacitors. Enter capacitance value so that it shows up on the schematic symbol. Otherwise leave blank.

- **Centroid Specified:**
  - If the part is non-symmetric and the datasheet does not provide a reference where to place the package outline select **NO.**
  - In all other cases select **YES**.
  - Examples: https://docs.google.com/drawings/d/1zfTWvPYSii7vjEup1B_k2rPJCzFeV4a0jqtArYFSkx4/edit?usp=sharing

- **Digikey Description:**
  - Search digikey for the part and find the part page. Copy the description and paste it into this attribute.
  - If the part doesn't exist on digikey try mouser and arrow.
  - If you still can't find this part on any distributor website then you can leave this attribute blank.

- **Digikey Part Number:**
  - Search digikey for the part and find the part page. Copy the digikey part number and paste it into this attribute.
    - If you can't find this part on digikey then you can leave this attribute blank.
    - If multiple Digikey part numbers exist use the **smallest** quantity number (usually cut tape).

- **Inductance**:
  - Used only for inductors. Enter the inductance value so that it shows up on the schematic symbol. Otherwise leave blank.

- **Mouser Partnumber:**
  - Search mouser for the part and find the part page. Copy the mouser part number and paste it into this attribute.
    - If you can't find this part on mouser then you can leave this attribute blank.
    - If multiple Mouser part numbers exist use the smallest quantity number (usually cut tape).

- **Octopart Partnumber:**
  - Leave this blank

- **Resistance**:
  - Used only for resistors. Enter the resistance value so that it shows up on the schematic symbol. Otherwise leave blank.

- **Temperature Range High:**
  - In the datasheet find the temperature range for the exact part number and then set this attribute to the high number.
  - Include the degree symbol ° and the unit of measurement, normally C for celsius.
    - Note: To add the ° symbol hold ALT and type 248 on a PC or press option + shift + 8 on a MAC.
  - Add a "+" or "-" for the temperature and don't include a space between the sign and the number (eg. +80°C)

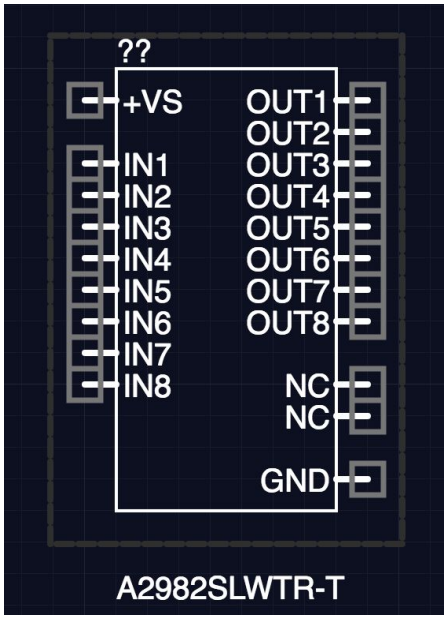
- **Temperature Range Low:**
  - In the datasheet find the temperature range for the exact part number and then set this attribute to the low number.
  - Include the degree symbol ° and the unit of measurement, normally C for celsius.
    - Note: To add the ° symbol hold ALT and type 248 on a PC or press option + shift + 8 on a MAC.
  - Add a "+" or "-" for the temperature and don't include a space between the sign and the number (eg. -25°C)

- **Voltage**:
  - Enter the voltage rating if applicable. Otherwise leave blank.

- **Custom Attributes:**
  - Other attributes need to be added that are part specific. These include attributes like:
    - Frequency
    - Current ratings
    - Max Vgs (mosfet)

        - Max Vds (mosfet)
        - Max Reverse Voltage (diode)
        - Idle current
        - Etc
    - When entering values do not place a space between the value and the unit (ex. 35V and 12uF)
    - The rule of thumb is to use the “Feature List” that is usually on the first page of the datasheet and think about what features or parameters from this list you might use to search for the part.
    - A good rule of thumb is to add at least 3 custom attributes.
    - We should only list attributes that are in the datasheet. If you notice any extra attributes that are not in the datasheet, delete them from the component.

Style Guide: Symbols



This section covers how to create a symbol now that you have configured the pins and the attributes.

Step by Step Walkthrough

1. ICs should have rectangular symbols - Click the handle unassigned pins button to automatically create a rectangular symbol and distribute the pins around it.

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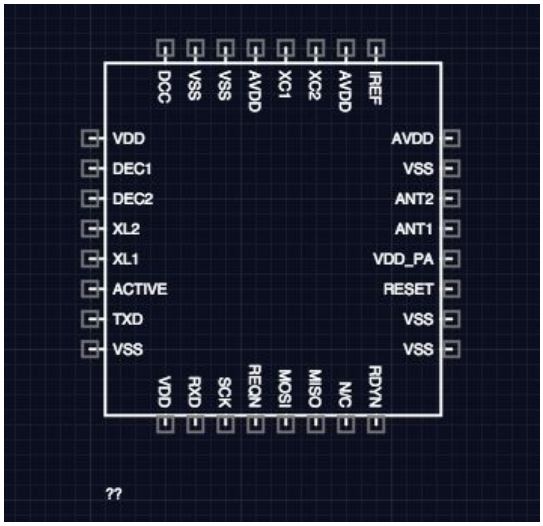
2. For connectors (headers, sockets, USB, etc) use the Handle Connector Male / Female buttons - this will automatically create the required symbol and style it like a connector for you.
    a. In the case of battery sockets such as CR2032 use the battery symbol and not the connector symbol.

3. For standard symbols (small components like resistors, diodes and transistors) use the Load Symbol dialog to automatically create the required symbol. Otherwise just make a rectangle.

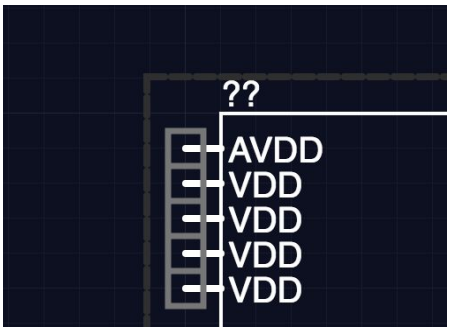
4. Pins are placed only on the Left and Right of the rectangle. Nothing on the top and bottom.

Good

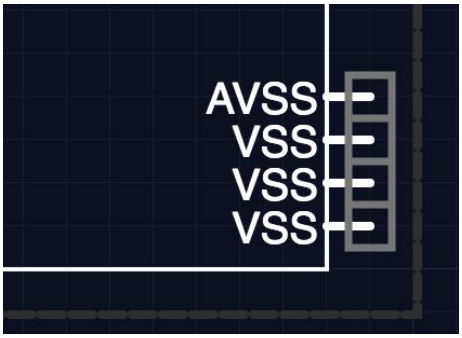


Bad

5. Power pins (anything with VDD/VCC in the name) go in the upper left corner of the rectangle, grouped by named in alphabetical order.

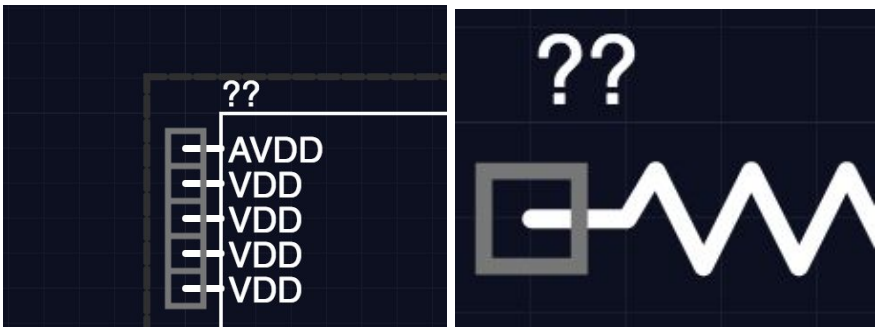


6. Ground pins (anything with GND/VSS) go in the bottom right corner of the rectangle, grouped by name in alphabetical order.

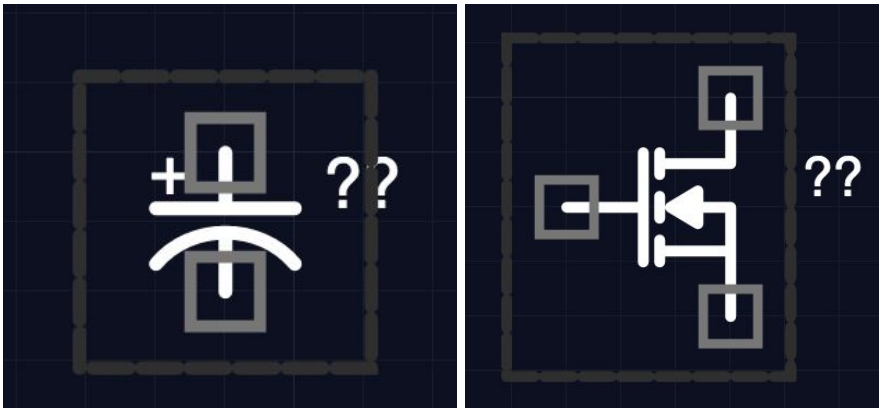


7. All pins must be represented on the symbol, including those that are No-Connects (NC). If there is a physical pin on the device **that connects to the PCB** there must be a corresponding pin on the symbol.
    - It is fine to have multiple pins with identical names if that's how it's specified in the datasheet (ie. multiple GND pins, or OUT pins, or COLLECTOR pins)

8. The location of the Refdes is determined by the type of symbol. You want to place it in such a way that it won't interfere with incoming connections:
    a. For IC's, Resistors, Inductors, Diodes, Transformers, Logic, Switches, Op Amps place the Refdes in the upper left corner



    b. For capacitors, batteries, transistors, mosfets, antennas, LED place the Refdes on the right side of the component.



9. For IC, Op Amp, logic, and transistors (if possible) place the part number in the lower left corner. You can make the part number visible from the part attributes page.

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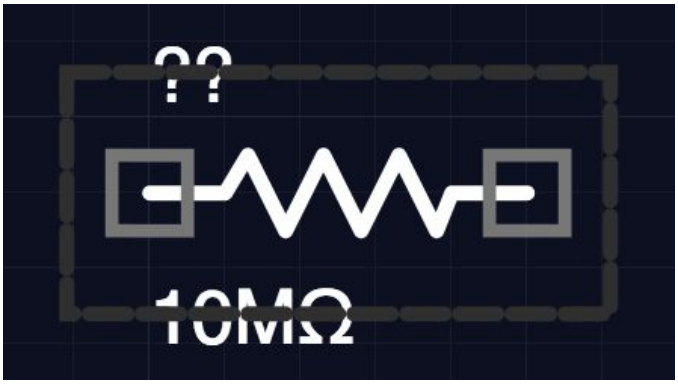
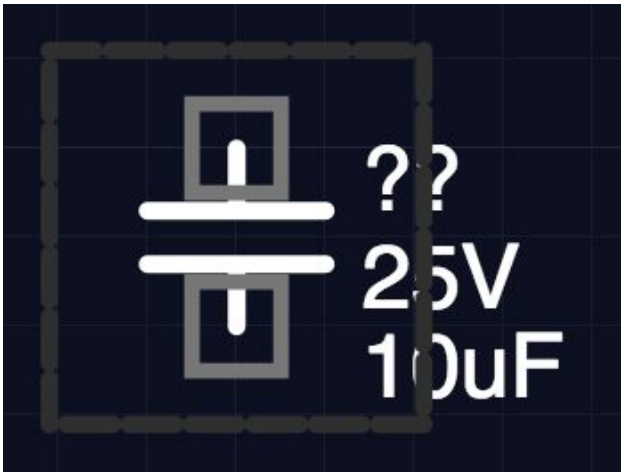
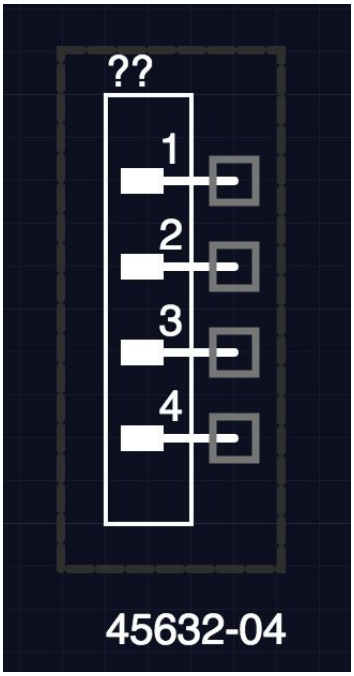
10. For resistors and inductors make the resistance and inductance value visible and place on the bottom left corner.



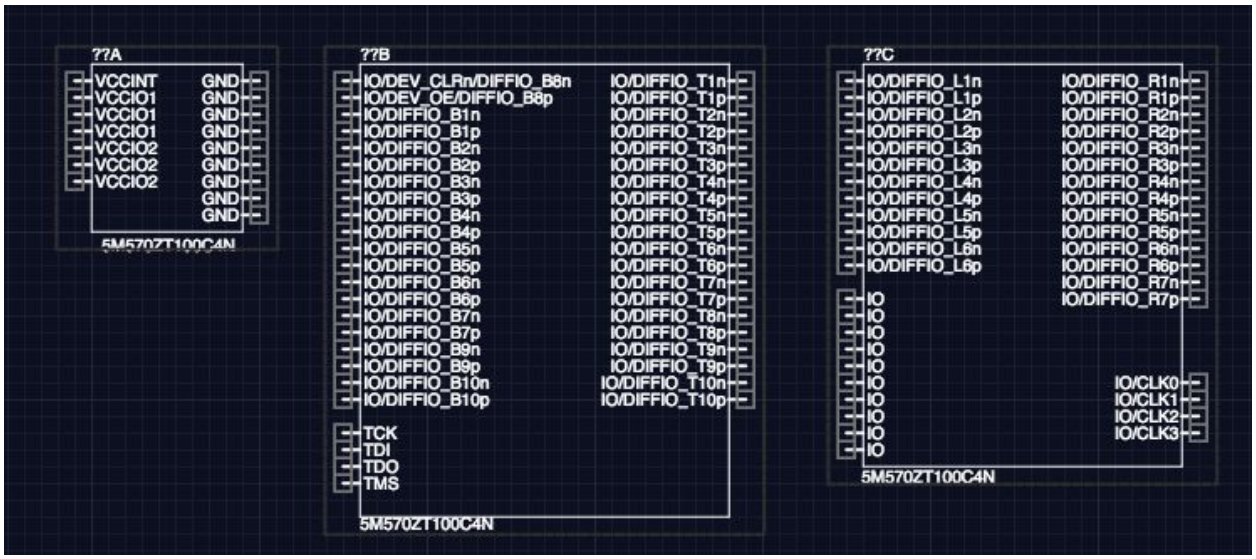
11. For capacitors make the capacitance and voltage value visible and place underneath the Refdes



12. For connectors, the pins must all be on the right side of the symbol. And leave one extra grid tick between pins so that there is enough room to hook everything up when drawing the schematic.



13. Use multi-part symbols for large devices (> 50 pins) to keep things organized.
    a. Break up the sub-symbols by major function.
    b. Have a separate symbol for power and/or ground.
    c. Try not to use too many sub-symbols. For large pin count parts the smallest sub-symbols should have at least 10 pins.
    d. Use best judgement on this as there is no exactly correct way.
    e. Each sub-symbol is named with the Refdes + a letter (eg. ??A, ??B, ??C)
        i. This is achieved by changing the Refdes text (when you double click on the symbol Refdes “??”) from {{refdes}} to {{refdes}}A and {{refdes}}B



14. Multipart symbols apply not only to large ICs but also to parts with multiple copies of the same standard part like resistor networks (ie. a 16-pin package containing 8 resistors).

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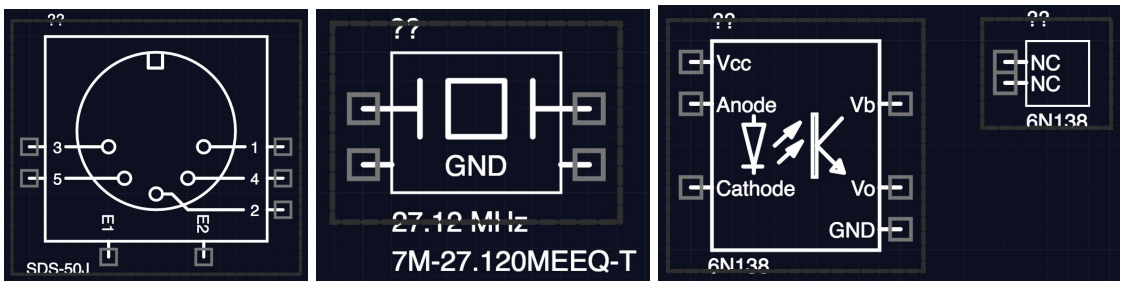
Resistor networks are often used for series termination on large busses. It's often cleaner to create a multi-part symbol where each part is a single resistor. This way, you can order the resistors on your schematic without nets crossing over when directly connecting them.

15. For simple parts it often makes sense to draw a functionality drawing inside the symbol. Components like level shifters, isolators, etc all benefit from these functionality drawings.



Headers

1. Headers are connectors, use the handle unassigned connector male or female button to generate this symbol.

2. Independent of header geometry outlined in the datasheet, all pins are to be placed on the right side of the schematic symbol.

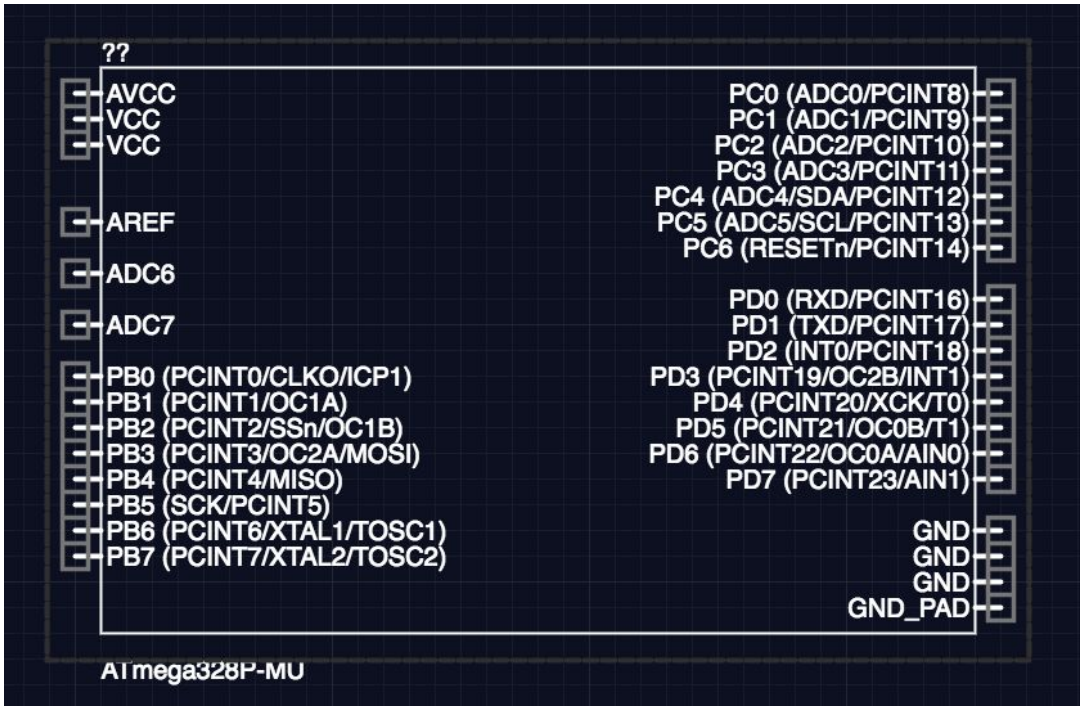
Pin Organization

1. The datasheet often has a "Typical Application" diagram that has a schematic symbol you should use as a reference. Group and position the pins closely to how it's shown while following the rules for VDD position, GND position, and having pins only on the left and right.

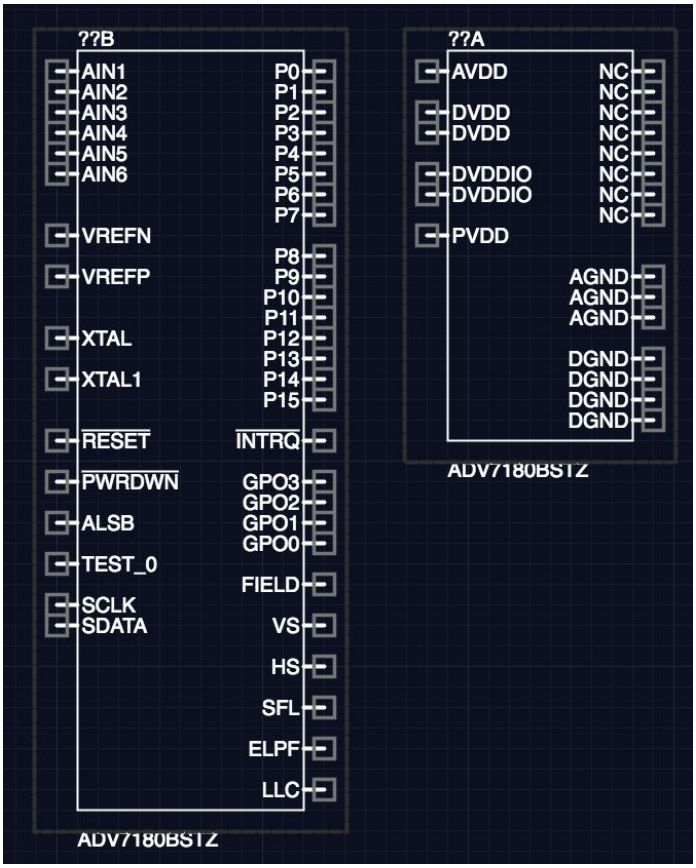
2. Copy the datasheet symbol for small symbol parts when the datasheet drawing seems to be reasonable.

3. Order and group pins on the symbols by function, not by number.
    - Pins within the same functional group will have zero grid spaces between them (ie. they will be side-by-side).
    - There should be 1 or 2 grid spaces between groups.

- In the example below you can see how the PB..7 signals are grouped together, PC0..6 signals follow PB and are grouped together, and PD0..7 come last and are grouped together.



- The example below shows proper groupings. Also inputs and I/O are kept on the left and outputs and I/O are kept on the right.



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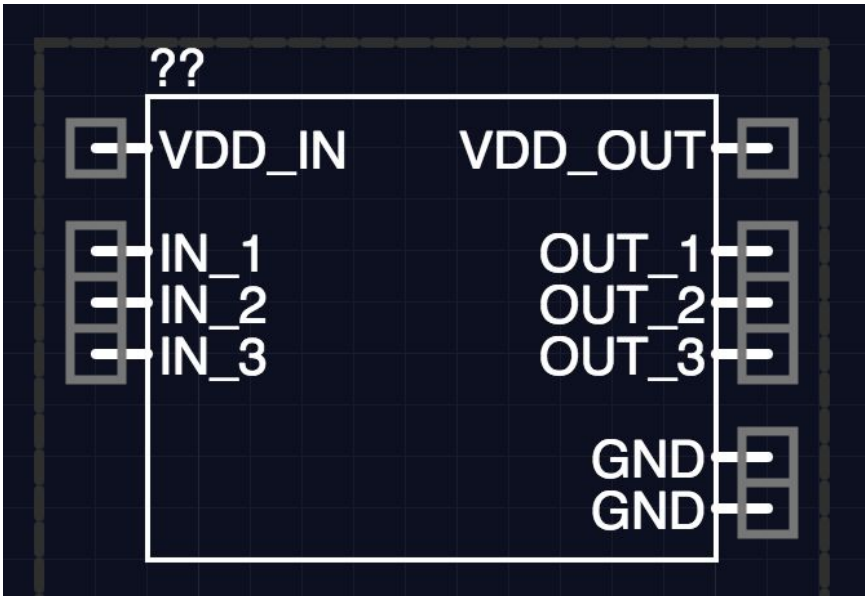
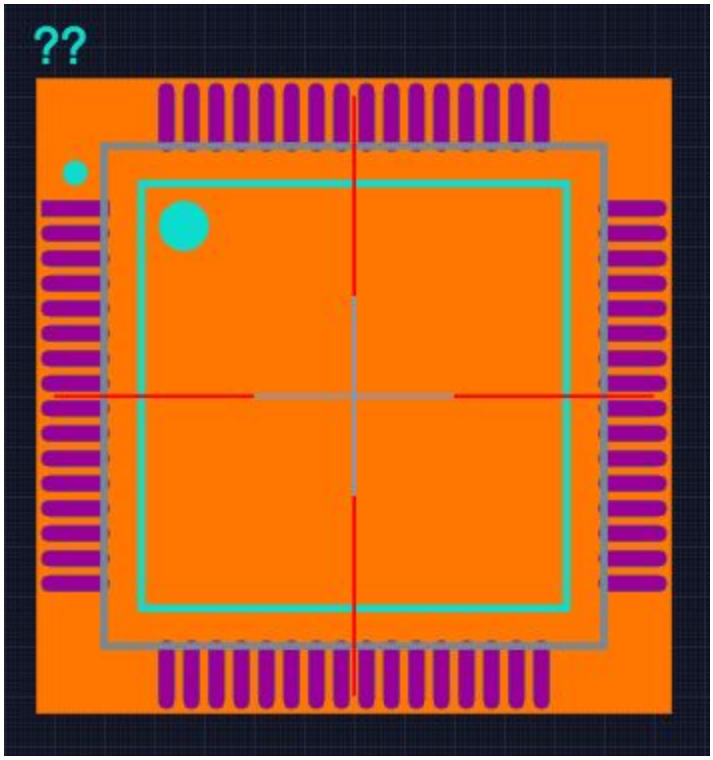
4. Data busses should not be split to different sides of the part.

5. For parts like level shifters it makes sense to break the VDD rules and split the symbol into input on the left and output on the right, including any output power supply voltage.



6. The goal is to create a verified, correct, and very reasonable and usable symbol. It's impossible to make a symbol that works perfectly in every user's schematic. If a user needs to move pins around to suit their personal schematic they will use our verified symbol as a starting point and edit it in their library.

Style Guide: Footprints



This section covers how to create a footprint now that you have configured the pins, attributes and the symbol.

General Tips

1. Use the footprint generator whenever possible (ie. for all standard footprints)
    - Always use Packing Level **C.** This will get you closest to the recommended footprint from the datasheet. Then adjust the result if the datasheet or manufacturer's website has a recommended footprint.

2. You will find that some non-standard footprints have similarities to standard footprints and you can use the generator to give you a head start.

3. If a part does not have a recommended footprint in the datasheets or a document on the MFG website but does have a footprint stack file (requires software like PADS or Eagle to open) then use the Upverter footprint generator. DO NOT USE THE FOOTPRINT STACK FILE. These are often not very high in quality or verified and a footprint using the footprint generator tool which follows IPC standards is more reliable.

4. Most connectors will have to be created manually

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5. Some datasheets have recommended footprints and those take priority over all other rules for creating footprints. Strive to get as close as possible to the recommendation.

6. When a datasheet provides multiple recommended footprints (for example: one for wave soldering, and another for reflow soldering) you always want to choose the most aggressive (ie. smallest) version which should be the reflow soldering version.

7. If a datasheet is lacking mechanical or footprint information, check the manufacturer's website for the part's product webpage to find more information.

8. You should almost never manually add shapes to copper or hole layers. Only use pad stacks and plated through holes.

9. When creating the package outline and silkscreen use a linewidth of 0.15mm unless it's a polarity marking silkscreen which needs to be 0.3mm.

Component Origin

1. Components must have their origin marked with two lines (one vertical and one horizontal) making a cross at the component origin (0, 0).

2. The component origin is given by the grid origin (0,0) in the footprint editor. The component origin must correspond to a flat surface on which the pick-and-place machine's suction cup can grab the component.

3. 99% of the time the origin will be the exact centre of the component package. A component's coordinates in the layout editor and in the exported pick-and-place (XY) file are specified with respect to its component origin.

4. Since many datasheets specify mechanical dimensions *relative* to physical points on the device, it can sometimes be tempting to use a component origin that is off-centre so that it's easier for you to use the datasheet dimensions directly when locating pad stacks. If you do this, make sure to move the finished part back to its proper centered origin or an appropriate flat pick-and-place surface before saving.

Layers

Top Component

1. This layer is used to position the part when placing via a pick-n-place machine. It is absolutely critical that the origin of the part be marked.

2. It shall have a red cross that exactly overlaps the component origin in the footprint editor at (0,0).

3. The footprint generator will create the centre cross automatically.

4. If you are **manually creating a footprint**, create a centre cross using the Add Line tool as follows:
    - The length of the first line shall match the smaller of the 2 dimensions of the Package Outline rectangle. For example, if the **Package Outline Width** is the smaller dimension, the first line shall be horizontal, pass through (0,0) and be as long as the Package Outline width. If the **Package Outline Height** is the smaller dimension, the first line shall be vertica, pass through (0,0) and be as long as the Package Outline height.

    - The second line shall be the same length as the first, but rotated 90 degrees so that a cross is formed.

    - Use an outline width of 0.04mm.

Top Package Outline

1. The package outline should exactly match the **nominal** dimensions of the component's body. The body does **not** include the pins or tabs. Should be a single rectangle / circle / semi-circle.

2. It is an **outline of 0.15mm** and should **not** be filled.

3. Think of the package outline as being used by PCB designers to roughly visualize the component bodies in 3D in their minds.

4. For circular components like axial capacitors the outline must be a circle.

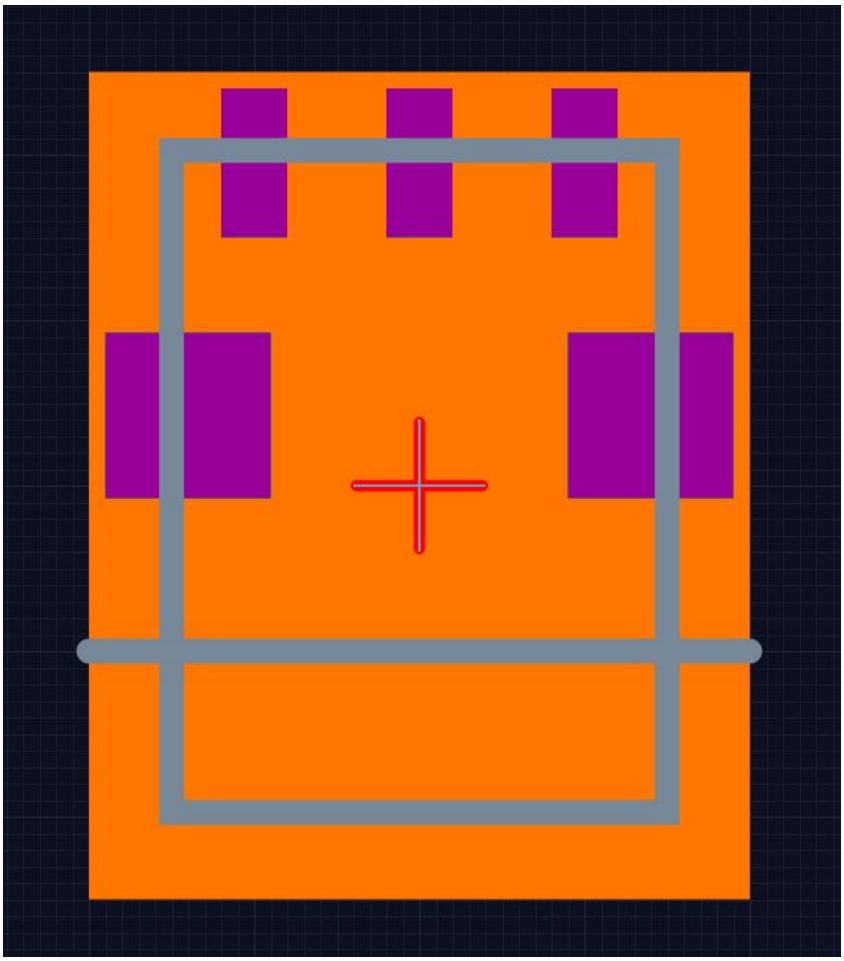
5. ~~For semi-circular components like TO-92 transistors the outline must be semi-circular.~~ **(Currently the tool cannot create arc shapes. Once this feature is added, this requirement will be reinstated)**

6. For irregularly shaped components, or components with notches cut out of them, draw a single rectangle to encompass the overall (nominal) dimensions. Important features (eg. heatsink tab on power fet) can be drawn in silkscreen.

7. When working with memory connectors that have memory cards (eg. SD Card) inserted, do not show the memory card location in silkscreen or package outline. The ejected card dimensions need to be included only in courtyard.

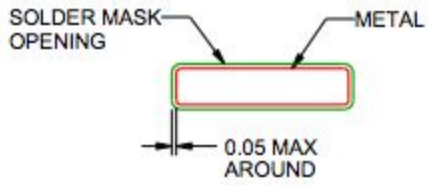
8. For DPAK style components please see the following document for proper placement of the origin cross and package outline: https://drive.google.com/open?id=1oEZO4fVwiZWfuDI2fq_oxmq2OQyYETaR2NmKwyaLJK4

9. For connectors that hang over the board edge, place a line that the PCB designer should use to align the connector to the board edge. The datasheet for such connectors generally have a recommend footprint that includes relative measurements from the board edge, so simply add a line to represent the board edge. Place this on the package outline layer. **The length of this line MUST equal the width of the courtyard. Line width = 0.15mm.**



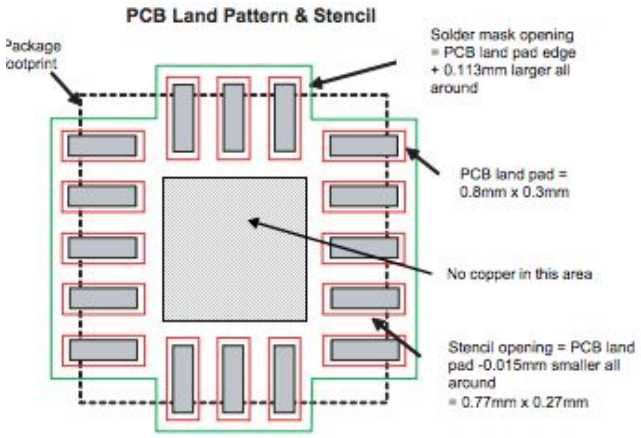
Top Solder Mask

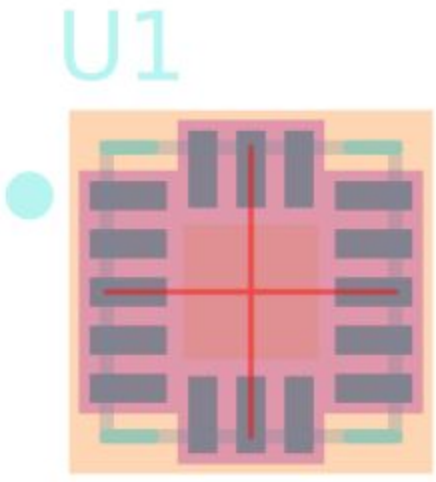
1. In 99% of cases do not implement the solder mask expansion recommended in the datasheet. This is aimed at parts that specify the solder mask expansion to be slightly bigger than the copper pads.
    a. Eg: Texas Instruments TAS6424-Q1



b. **The solder mask layer will identically match the copper layer. All soldermask expansion or reduction is handled in the export tools**.

2. There are exceptions where solder mask expansion needs to be implemented. These cases have unique solder mask requirements. Below is an example:



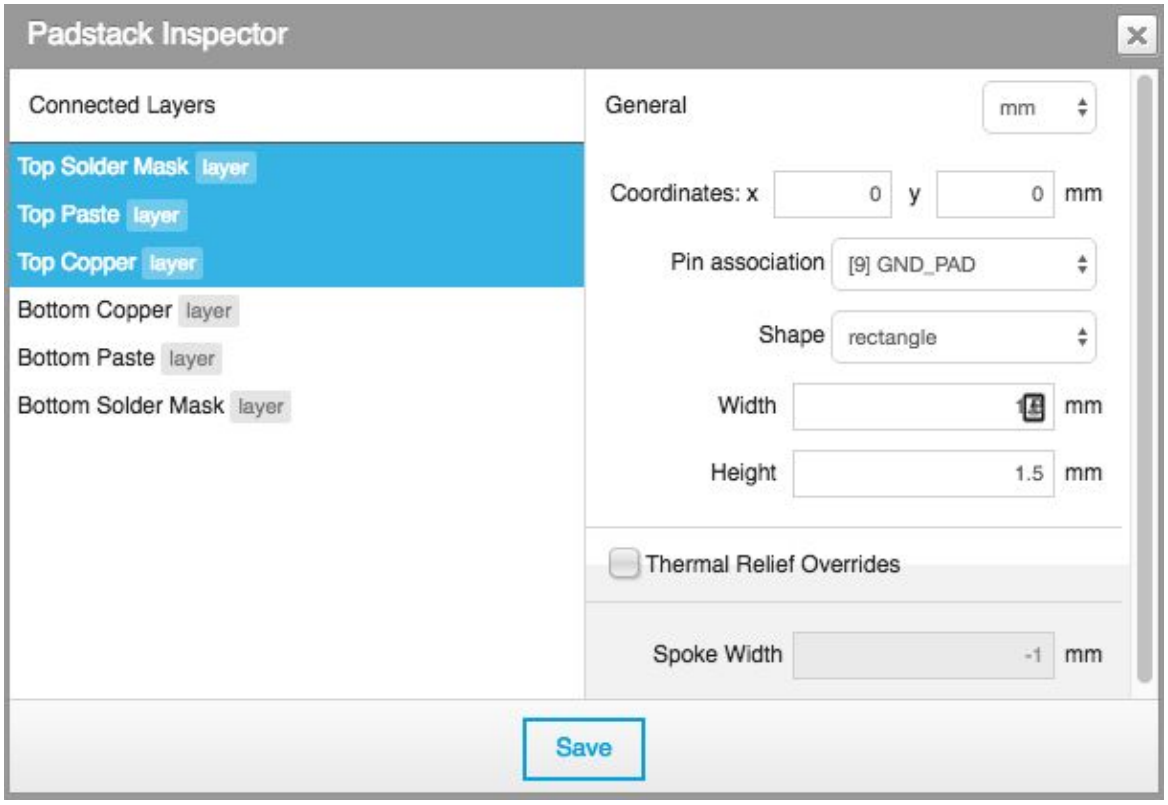


a. The part above requires the whole area under the pads to be free of solder mask. In these cases, the solder mask design needs to be implemented.

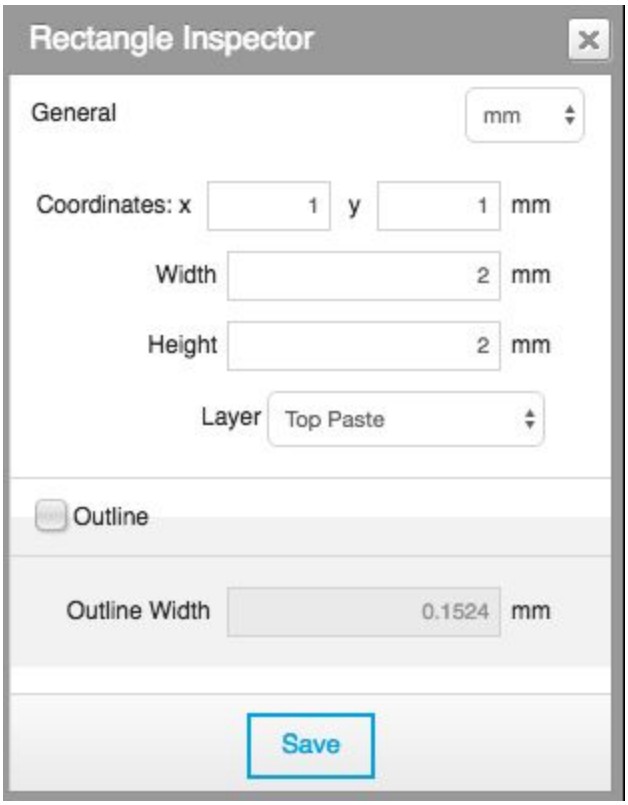
Top Paste Mask

1. There is generally nothing to do here. The Paste Mask layer will be generated automatically through the use of the Generator, Padstack, or Hole tools in the footprint editor.

2. Thermal pads are commonly used on standard footprints so the footprint generator can be used. It defaults to a 40% paste coverage, which means the paste mask opening is reduced relative to the copper pad. This all happens automatically.
   - **An exception is if the datasheet asks for a special paste mask design** (sometimes called a 'stencil' design) for a thermal pad. It might ask for a 2x2 or 3x3 'window' pattern.
   - **To create manual paste mask design follow these steps**:
     1. Open the pad properties window for the pad that requires a special paste mask design.



2. Unselect the Top Paste so it's not highlighted and press Save.
3. Open the Rectangle Draw tool and draw the Special Paste Mask Design by selecting the Top Paste Layer:



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- **The generator automatically implements windowing for thermal pads larger than 5x5mm**, so keep that in mind.

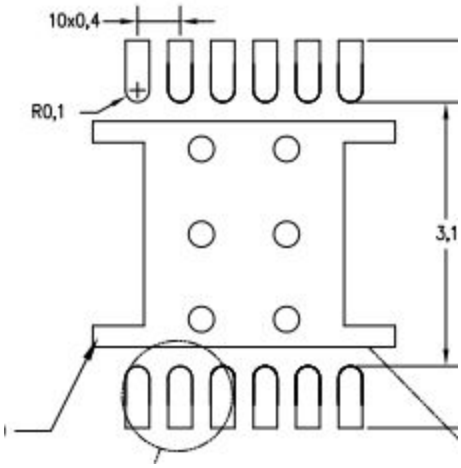
3. The datasheet may also specify a special stencil design for other pads (not just thermal pad) and you must follow those.

Top Copper

1. Copper pads must be created through the use of the Generator, Padstack, or Hole tools only.

2. Use Rounded Rectangle pad shapes unless otherwise specified in the datasheet.

3. If the datasheet specifies a recommended footprint with pads that are rectangular on one side and rounded rectangular on the other side as shown in the picture below, make them completely rectangular in Upverter.



4. Pin-1 should be a ‘Rectangle’ shape as a way to indicate that it’s Pin-1 unless otherwise specified in the datasheet.

5. Pad coordinates must exactly match the datasheet.

6. Pad sizes (width, length, rounding angle, etc) must exactly match the datasheet.

7. The footprint generator is not perfect. You must use the Measure tool to double check the output against the datasheet, especially if the datasheet has a recommended footprint. Tweak the generator parameters to match the recommended footprint as closely as possible. Some areas where the generator may go wrong are:

Top Courtyard

1. If you need to create a courtyard manually, the courtyard shall be 0.1mm longer on each side than the **COPPER PADS or the MAXIMUM PART BODY, WHICHEVER IS**

BIGGER. Remember the part outline is based on nominal part dimensions and the courtyard must be based on **MAX PART BODY** dimensions.

a. Refer to the following document for examples: https://docs.google.com/drawings/d/1tM8cvJ6Ox40l1UJNr8xrbzc1sy5va-rAbZNvuisv0IE/edit?usp=sharing
b. In the rare case where the datasheet does not provide maximum dimensions or tolerances and only the nominal dimensions are available, then use the nominal dimensions for the courtyard calculation.

2. Use the Rectangle tool to create a filled-in rectangle.

3. If the part is circular then the courtyard should be a circle too.

4. ~~If the part is a semicircular then the courtyard should be a semicircle too.~~ **(Currently the Upverter tool cannot create arc shapes. Once this feature is added, this requirement will be reinstated)**

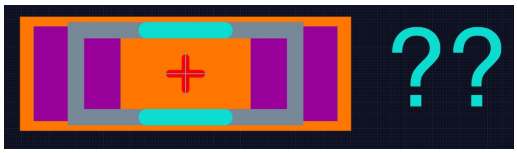
5. If the part is an odd circular/semicircular shape that cannot be created exactly using the arc / circle tools or necessary dimensions are not provided then make a rectangular / square courtyard.

6. When working with memory connectors that have memory cards (eg. SD Card) inserted, include the ejected card dimensions in the courtyard. Do not show the memory card location in silkscreen or package outline.

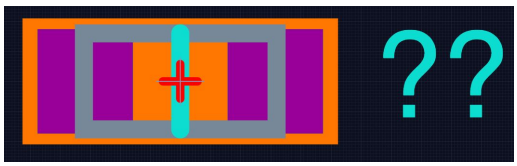
Top Silkscreen

1. Create an outline with dimensions as close as possible to the package outline. This sometimes means going outside the pins, the sometimes means going inside the pins. Use your best judgement and put the silkscreen as close as possible to the outline. The line width should be 6Mil (0.15mm)

2. As resistors and capacitors get smaller you'll need to change the way you draw their silkscreen. At their biggest, the silkscreen should look like a rectangle where the pads have been cut out (so two lines one at the top, and one at the bottom).



Next down it should look like a vertical line between the two pins.



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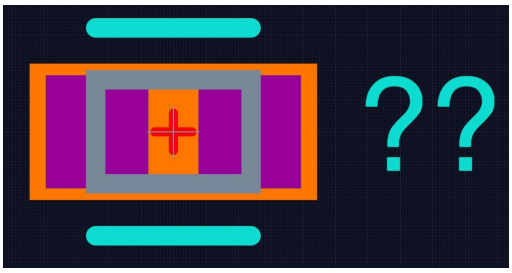
Finally at the smallest size, it should look like two lines outside the component, one on the top and one at the bottom.



3. You can often use the rectangle tool, but if the outline is circular, ~~semicircular~~, or irregular you must follow the outline instead.

4. If the part is small, or irregularly shaped try to match the outline as closely as possible to the outline leaving gaps for pins.

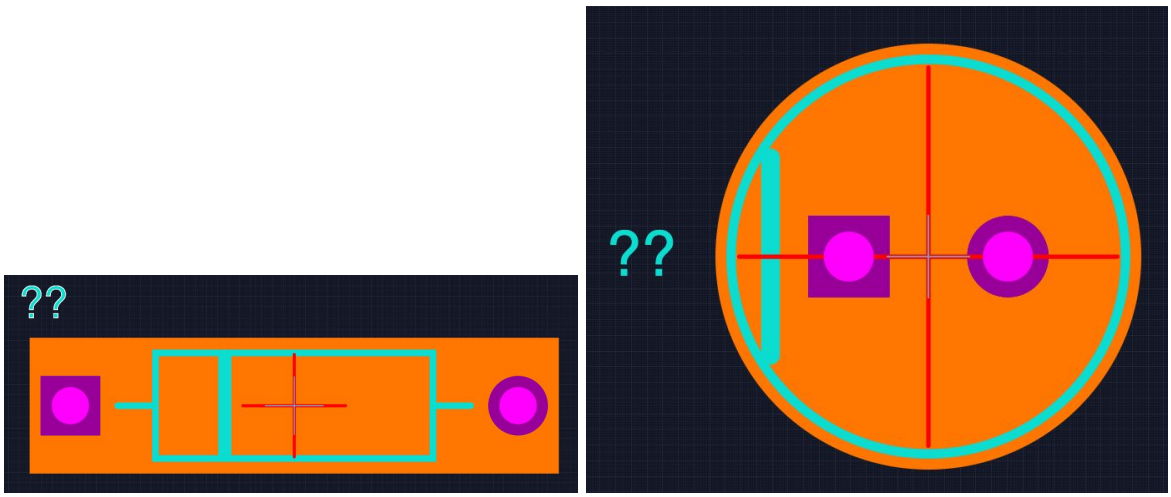
5. Silkscreen must be at least 0.3mm clearance from all copper pads (edge of copper to edge of silkscreen line).

6. Silkscreen must be at least 0.15mm clearance from all other silkscreen (edge of silkscreen line to edge of silkscreen line).

7. For parts with at least 4 pins add a filled-in circle of radius 0.25mm beside Pin-1, **outside** the silkscreen outline. The exact location is not crucial as our verifier can handle this.

8. **Polarity Markings if the datasheet does not name the pins or names PIN 1 the cathode and PIN 2 the anode**:

    a. For small parts that do not have a polarity marking on the physical part body or small parts that have a cathode (negative) polarity marking on the body:
        i. Set Pin-1 to be the cathode (negative terminal) and Pin-2 to be the anode (positive terminal)
        ii. Add a filled-in circle of radius 0.25mm beside Pin-1, **outside** the silkscreen outline to mark the cathode
    b. For larger parts that do not have a polarity marking on the physical part body or large parts that have a cathode (negative) polarity marking on the body
        i. Set Pin-1 to be the cathode (negative terminal) and Pin-2 to be the anode (positive terminal)
        ii. Mark the negative polarity (cathode) of the part with a thick (>0.3mm) silkscreen line on the inside of the part next to the cathode (remember silkscreen must be >0.3mm away from the pad)



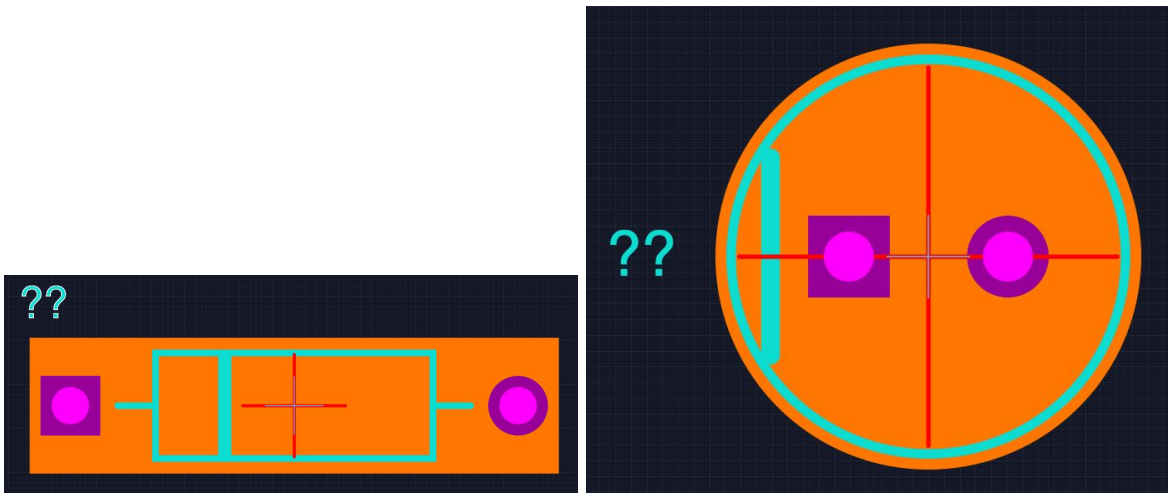
c. For large parts that have an anode (positive) polarity marking on the body
    i. Set Pin-1 to be the cathode (negative terminal) and Pin-2 to be the anode (positive terminal)
    ii. Mark the **positive** polarity (anode) of the part with a thick (>0.3mm) silkscreen line on the inside of the part next to the anode (remember silkscreen must be >0.3mm away from the pad)
    iii. This is rare and will mostly occur with tantalum capacitors

d. THIS IS A RARE EXCEPTION: In the rare case that you are working on a small part that has an anode (positive) polarity marking on the body
    i. Set Pin-1 to be the cathode (negative terminal) and Pin-2 to be the anode (positive terminal)
    ii. DO NOT ADD a filled-in circle of radius 0.25mm beside Pin-1
    iii. Create a plus "+" silkscreen symbol and place near the anode

9. **Polarity Markings if the datasheet names PIN 1 the anode and PIN 2 the cathode**:

a. For small parts that do not have a polarity marking on the physical part body or small parts that have an anode (positive) polarity marking on the body:
    i. Set Pin-1 to be the anode (positive terminal) and Pin-2 to be the cathode (negative terminal)
    ii. Add a filled-in circle of radius 0.25mm beside Pin-1, **outside** the silkscreen outline to mark the anode

b. For large parts that have an anode (positive) polarity marking on the body
    i. Set Pin-1 to be the anode (positive terminal) and Pin-2 to be the cathode (negative terminal)
    ii. Mark the **positive** polarity (anode) of the part with a thick (>0.3mm) silkscreen line on the inside of the part next to the anode (remember silkscreen must be >0.3mm away from the pad)



c. For large parts that have a cathode (negative) polarity marking on the body
    i. Set Pin-1 to be the anode (positive terminal) and Pin-2 to be the cathode (negative terminal)
    ii. Mark the **negative** polarity (cathode) of the part with a thick (>0.3mm) silkscreen line on the inside of the part next to the anode (remember silkscreen must be >0.3mm away from the pad)

d. For larger parts that do not have a polarity marking on the physical part body or small parts that have a cathode (negative) polarity marking on the body
    i. Set Pin-1 to be the anode (positive terminal) and Pin-2 to be the cathode (negative terminal)
    ii. DO NOT ADD a filled-in circle of radius 0.25mm beside Pin-1
    iii. Create a plus "+" silkscreen symbol and place near the anode.

10. Do not mark pin 1 in any other way (plus, or C for cathode, etc).

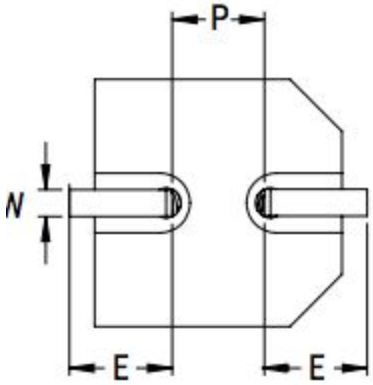
11. Be sure the refdes is visible and placed in the top left corner, outside the silkscreen rectangle. The generator will create the refdes automatically. If you need to manually create it, use the Text tool and set the Text field to {{refdes}} and a Font Size of 1mm.

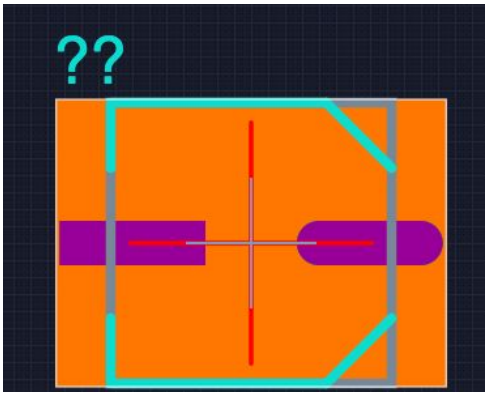
12. Add any other text or shapes that might be useful.

13. When working with board edge components such as connectors, do not place any silkscreen within 0.5mm of the board edge line and no silkscreen past the board edge line.

14. When working with memory connectors that have memory cards (eg. SD Card) inserted, do not show SD Card location in silkscreen or package outline. The ejected card dimensions need to be included only in courtyard.

15. If the part has a cut corner like shown below, the silkscreen needs to include the cut corner as well using datasheet dimensions. If dimensions are not provided, make the corner cut 1mm x 1mm. If that size is too large for the symbol (causes silkscreen to pad spacing violation) use 0.5mm x 0.5mm.





Top Keepout

1. Generally left blank.

2. Some components like antennas and wireless modules specify a keepout region (ie. a region on which there shall be no copper). Create a filled-in rectangle in the appropriate spot if needed.
    a. Do not include solder keepout areas. Only draw copper keepout areas.

Bottom Layers

1. Generally nothing is needed for the bottom layers as long as you used the Generator, Padstack, or Holes tool to create every pad.

2. Some parts (mostly board edge connectors) require copper or keepouts on the bottom layers. If the part calls for pads on the bottom of the board, or a keepout, you must add it to these layers.

Mechanical Details, Rulers, Notes, Design Rules

1. Nothing needs to be added to these layers unless the datasheet calls for non plated rounded rectangular shaped slots. For non plated rounded rectangular slots use the rectangle tool with a corner radius that's specified in the datasheet. Select the Mechanical Details layer and make sure outline is not selected.

Hole Layer

1. Nothing extra is needed since it will be taken care by the Add Hole tool.

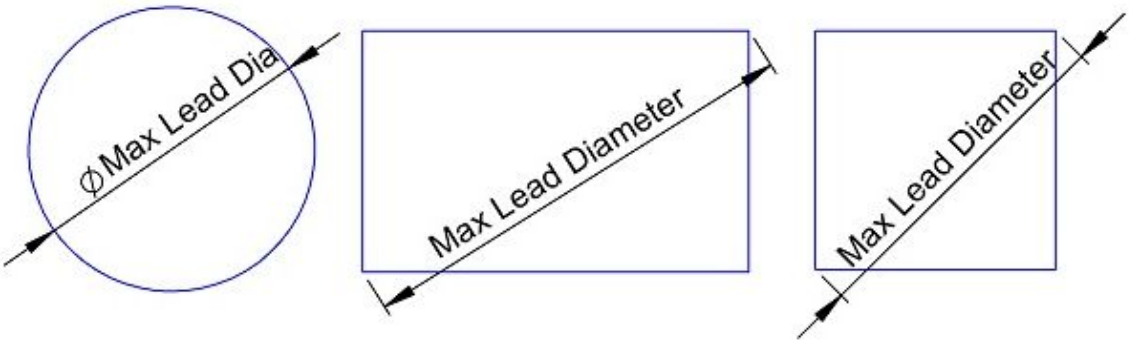
Hole Sizing

Taken from http://www.pcb-3d.com/knowledge-base/pth-dimensions

Plated Through Holes

1. Pin-1 should have a square-shaped pad

2. **Many datasheets will tell you what hole dimensions to use. If they don't, follow these guidelines:**
    a. **Internal hole diameter = (maximum diameter of lead + 0.15mm) rounded up to 0.05mm (eg. 1.323mm becomes 1.35mm)**
        i. **For leads that are not circular maximum diameter = hypotenuse = square root (length^2 + width^2)**



    b. **Plating ring diameter = [Internal hole diameter] + 0.5mm for max lead diameter up to and including 0.8 mm, +0.05 mm for every 0.1mm (rounded up) above 0.8 mm.**

    c. **The hole sizes we specify are for finished holes. The manufacturer will increase all hole sizes to account for plating and we don't need to worry about it.**

3. If the datasheet has a recommended footprint and specifies the hole size, then follow the datasheet for the hole size. If the datasheet has a recommended footprint and specifies the plating ring diameter, then follow the datasheet for the plating ring diameter. If the datasheet has a recommended hole size but does **NOT** specify a recommended plating ring diameter then use the plating ring diameter rule (2b) with a **max lead diameter = recommended hole size - 0.15mm**.

4. If the datasheet has a plated rectangle hole in the recommended footprint, make a plated slot that fits the entire rectangle inside with a plating ring diameter = length or width + 0.6mm.

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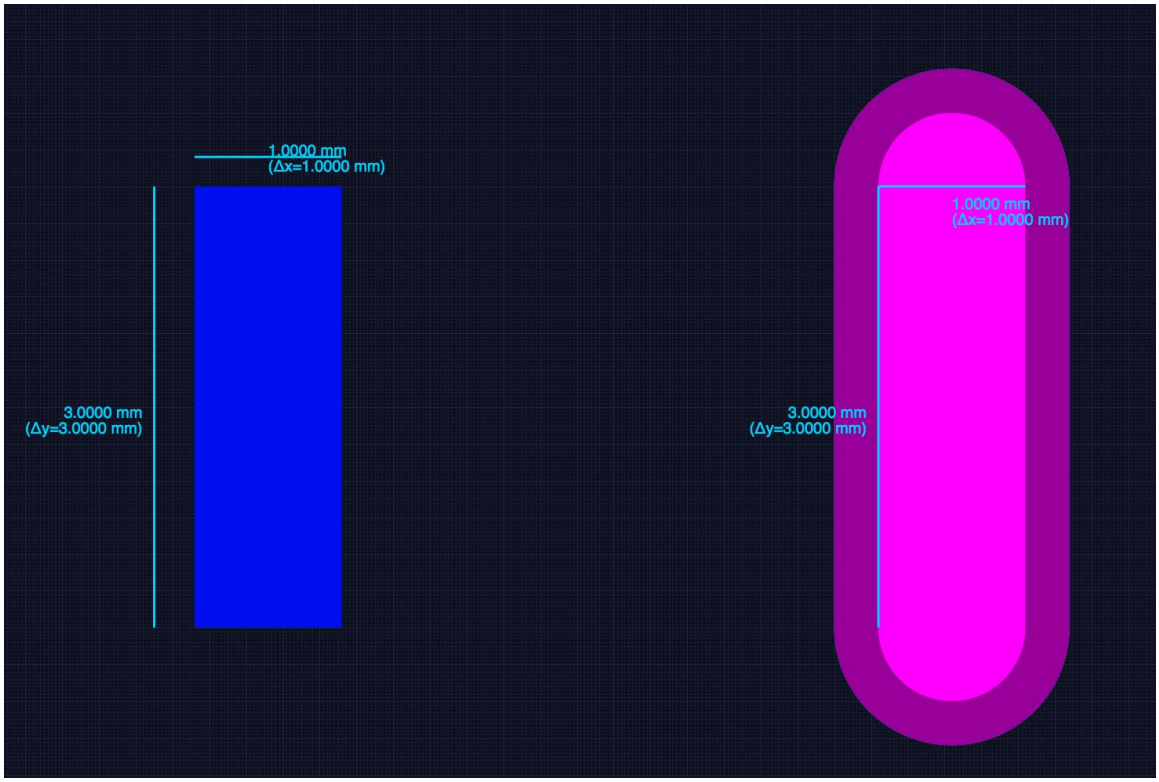
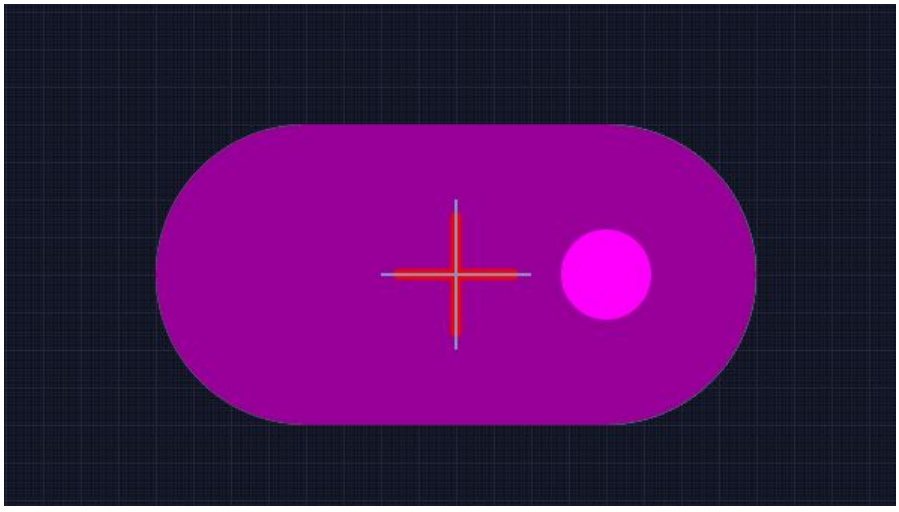
a. In the example below, the recommended footprint requires a plated rectangle hole that is 1mm x 3mm (left). The implementation is on the right.



5. To make oblong pads with offset plated through holes use the following rules:



a. Using the new padstack tool make an oblong pad and associate it with the required pin name.
b. Using the through hole inspector make the plated through hole. Use the hole diameter as specified in the datasheet. The plating diameter = the height of the oblong pad. You want the plating of the through hole to be the same size as the oblong pad thickness. **Then associate the through hole with the required pin name as well**.

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TO-92 and Other Parts With Overlapping Holes/Pads

1. The above IPC rules result in overlapping holes and pads for some components. If the datasheet or product webpage doesn't have a recommended footprint, we will use the following rules.

2. **Internal hole diameter = maximum diameter of lead + 0.15mm (the oversize corresponds to Level-C packing)**

3. **Plating diameter = Internal hole diameter + oversize (where oversize is 0.5mm if at least 6 mils (0.1524mm) clearance between pads is available, if not reduce oversize until 6 mils clearance between pads). If you need to reduce the plating ring diameter to meet the 6 mils clearance then round the diameter down to 2 decimal points (1.346mm becomes 1.34mm, 1.2mm stays at 1.2mm).**

Non Plated Through Holes (NPTH)

1. Internal hole diameter = whatever the datasheet says.

2. For non plated slots that are rounded rectangular in shape use the rectangle tool with a corner radius that's specified in the datasheet. Select the Mechanical Details layer and make sure outline is not selected.

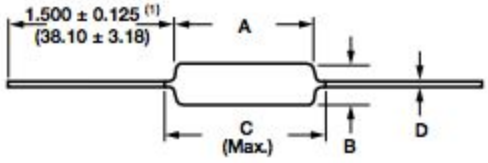
Axial Components

1. Taken from IPC-7251

2. Centre-to-centre spacing between the 2 holes = Max body length + (2 * lead_extension)

Max Lead Diameter (mm)	**lead_extension (mm)**
0.2 - 0.8	1.0 **+** max_lead_diameter (that's a plus sign)
0.85 - 1.20	3.3 ***** max_lead_diameter (that is multiplication)
> 1.25	4.4 ***** max_lead_diameter (that is multiplication)

- Note: In cases where two body lengths are shown as in the example below, dimension C should be used for the max body length:



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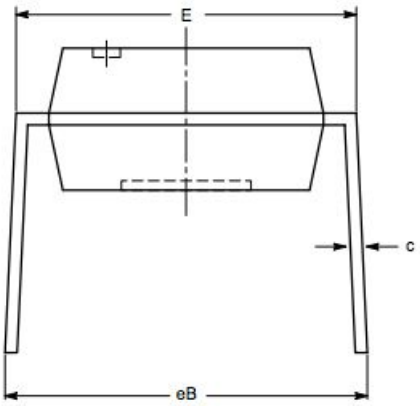
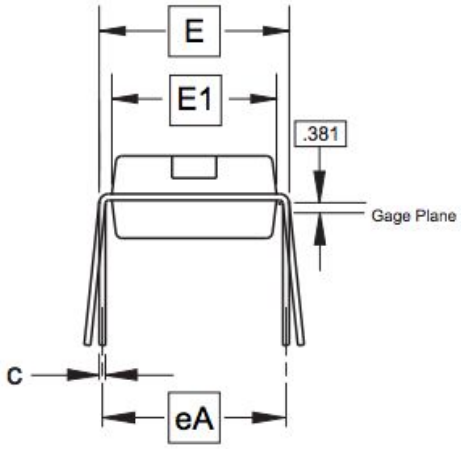
DIP Components

1. If no recommended footprint exists in the datasheet or MFG website, centre-to-centre spacing between the 2 columns of holes = dimension E from the mechanical drawing (not eB/eA). If E is not provided use eA, centre of pin to centre of pin, or eB - c.





Thermal Pads

1. Vias:
    a. If the datasheet specifies a via in thermal pad requirement then include them in the footprint. **The datasheet must provide a minimum number of vias as the minimum information. If this is not present then do not add vias to your footprint.**
    b. Via Diameter:
        i. If the datasheet specifies a via diameter use the specified diameter (if range is specified, use smallest)
        ii. If the datasheet does not specify a via diameter use 0.3mm internal diameter.
    c. Via Pad Diameter:
        i. If the datasheet specifies a via pad diameter use the specified diameter (if range is specified, use smallest)
        ii. If the datasheet does not specify a via hole size or pad diameter use 0.6mm pad diameter.
        iii. If the datasheet specifies a via hole size but not a pad diameter then pad diameter = 0.3mm + via internal diameter.
    d. Via Spacing:
        i. If the datasheet specifies the via spacing use the specified spacing in your footprint (if range is specified, use nominal)

ii. If the datasheet does not specify via spacing then arrange in an evenly spaced grid. (Eg. Thermal Pad = 5mm x 5 mm, 9 via requirement. Create a 3x3 via grid with spacing = 5mm / (3 vias +1) = 1.25mm spacing)

BGAs

Use the BGA Configuration Tool to create the footprint.

1. Make sure all of your pin names are entered into the pin table before using the BGA footprint tool. The tool with automatically associate the pin names to the pads.
    a. NOTE: Make sure that your pin name style matches the BGA tool style choice (Alphabetic, Numeric)
    b. Make sure the “Letters to skip” field contains all the letters that are skipped in the datasheet pin naming.

2. All dimensions entered into the BGA footprint tool should be nominal.

3. Select packing level C.
4. The radius dimension entered into the “Padstack” section of the BGA tool refers to the nominal BGA ball radius specified in the datasheet.

5. If the datasheet has a recommended solder mask expansion, enter this value into the solder mask expansion field in the BGA tool.
    a. NOTE: Often times the datasheet will identify two options: 1. Solder mask defined (SMD) and 2. Metal Defined (MD). Follow the metal defined option.

6. Press save and verify that the pins were properly mapped to the pads.

7. If the datasheet provides a recommended footprint, adjust the output from the generator to match the recommended pad sizes.
    a. NOTE: Some datasheets don’t directly identify the copper and paste mask dimensions and instead use SR/SP/SL. Take a look at this example on page 82: http://www.nxp.com/documents/data_sheet/LPC1769_68_67_66_65_64_63.pdf
    b. SR = occupied area - This is the nominal size of the ball
    c. SP = solder land - This is the size that you want to make the copper pads
    d. SL = solder paste deposit - This is the size that you want to make the paste mask

Additional Guidelines

The following section is mostly designed for Upverter Part Specialist marketplace contractors. It covers common part creation errors, and specific suggestions for each of the different kinds of parts they may need to work on.

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Common Mistakes Made

The following is a list of the errors we see parts contractors make most frequently. Please read this list and try to keep it in mind when you're making parts - it will help you keep your ratio high!

Missing refdes (both symbol and footprint)

Every part must have a reference designator both in the symbol and in the footprint. The symbol refdes will look like "??" and should be placed near pin one. Though make sure it's at least 0.3mm clearance from any pad and 0.15mm clearance from other silkscreen.

Holes not big enough (exact size of the hole)

Make sure when you create holes that you correctly account for the size of the pin and the thickness of the plating.

The datasheet is for a different part

One of the first things you should do is double check that the datasheet matches the part number requested. If the datasheet is wrong or empty you will have to go and find the right one and update that attribute.

No part number on IC schematic

Non-passives and parts with more than 2 pins should have a part number as part of their schematic symbol. It should be there by default, but if it gets removed you can turn it on in the attributes editor.

No keepouts (this came up with antennas)

Every part needs to have at least a component courtyard (orange), and in the case of transmitters, antennas, some modules and some other parts it should also have top and bottom keepouts. These will be specified in the datasheet, make sure you add them to the footprint.

Ground or power pins on the top or bottom of a symbol

Pins should never be added to the top or bottom of a symbol. Only use the left and right. Inputs should be on the left, outputs on the right.

No pin one marker (footprint)

Pin one must be marked for parts with 4 or more pins, and for most lower pin count parts with polarity. In some cases polarity is marked with a thick line. See the specific instructions below for the exact part you're making.

Footprints not centered

The footprint should be centered at 0,0. There are some cases where connectors are easier to create using a different origin, but even in these cases the finished part should be moved to 0,0 before saving.

Missing mechanical details or holes on the wrong layers

Mechanical details like cuts and slots need to be created on the mechanical layer. Holes need to be created on the hole layer. Never use outlines, or draw circles instead of using the hole tool.

Wrong number of pins

Lots of users have been confused by the number of pins in some mechanical parts. The rule of thumb for this is to add one extra pin for the housing and associate this pin with all of the pads the housing gets soldered to.

Bad pin names

Pins need to be named exactly like they are in the datasheet. If they aren't named then follow the rules of thumb laid out in the Pin Names section.

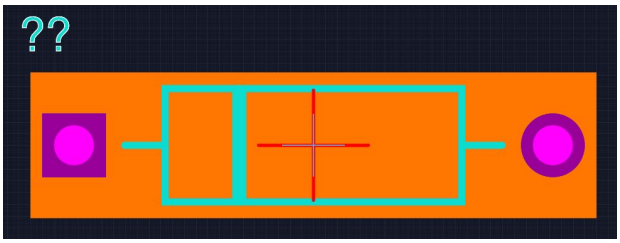
Missing overbars or # or n in the pin name

When you copy pin names the over bar does not come with it. You need to edit the pin name and add a ! in the front of it. If a pin name ends in a lowercase n or includes a # you need to delete those characters from the pin name and put a ! at the start.

Marking pin one improperly

Do not mark pin 1 with anything other than a polarity marker or a filled circle. Users have been adding "+" and "C" to capacitors to mark the CATHODE (PIN 1) - this is wrong.

Specific Guidelines for Axial Components

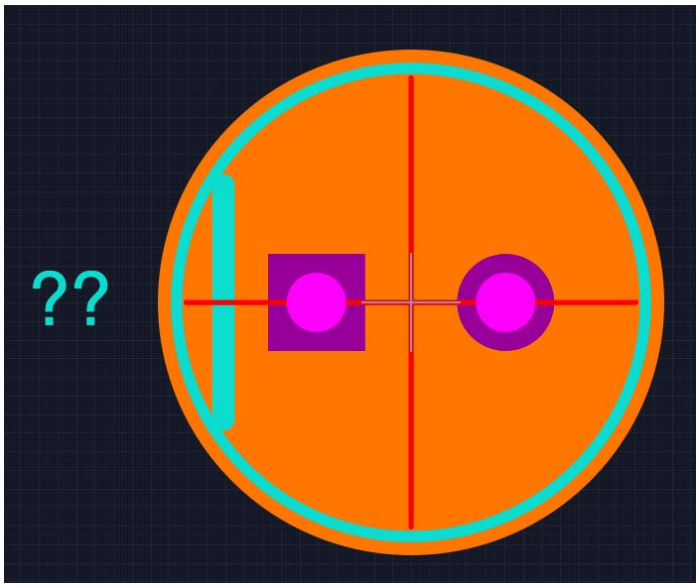


Axial leads protrude from each end of a typically cylindrical or elongated box-shaped component, on the geometrical axis of symmetry. Axial-leaded components resemble wire jumpers in shape, and can be used to span short distances on a board, or even otherwise unsupported through an open space in point-to-point wiring. Axial components do not protrude much above the surface of a board, producing a low-profile or flat configuration when placed "lying down" or parallel to the board.

Things to watch out for:

- No pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- Mark the polarity of the part with a thick (>0.3mm) silkscreen line.
- The component outline (grey) should only mark the size of the body of the part (beneath the silkscreen in the picture above).
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.
- Add little silkscreen lines to indicate where the leads of the part will go.
- Name the pins exactly as they are in the datasheet, if there are no names and the part has polarity use CATHODE (PIN 1) and ANODE (PIN 2), otherwise use 1 & 2.

Specific Guidelines for Radial Components

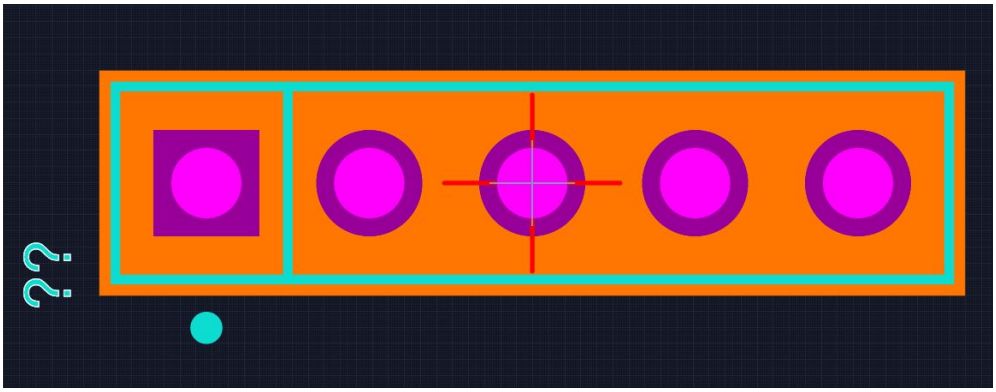


Radial leads project more or less in parallel from the same surface or aspect of a component package, rather than from opposite ends of the package. Originally, radial leads were defined as more-or-less following a radius of a cylindrical component (such as a ceramic disk capacitor). Over time, this definition was generalized in contrast to axial leads, and took on its current form. When placed on a board, radial components "stand up" perpendicular, occupying a smaller footprint on sometimes-scarce "board real estate", making them useful in many high-density designs. The parallel leads projecting from a single mounting surface gives radial components an overall "plugin-nature", facilitating their use in high-speed automated component insertion ("board-stuffing") machines.

Things to watch out for:

- No pin one silkscreen dot.
- The courtyard, outline, silkscreen, etc should all be circular NOT rectangular.
- Unless specified differently in the datasheet, make the pin one pad square.
- Mark the polarity of the part with a thick (>0.3mm) silkscreen line.
- The component outline (grey) should only mark the size of the body of the part (beneath the silkscreen in the picture above).
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.
- Name the pins exactly as they are in the datasheet, if there are no names and the part has polarity use CATHODE (PIN 1) and ANODE (PIN 2), otherwise use 1 & 2.

Specific Guidelines for Header Components



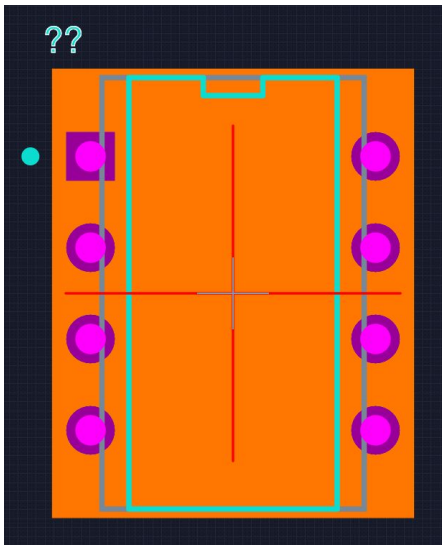
(rotated)

A pin header (or simply header) is a form of electrical connector. It consists of one or more rows of male pins typically spaced 2.54 millimetres (0.1 in) apart. The distance between pins is commonly referred as pitch in the electronic community.

Things to watch out for:

- Use a pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- If pitch allows (> 0.7mm), mark the polarity of the part by boxing pin one with silkscreen.
- Name the pins exactly as they are in the datasheet, if there are no names use numbers starting with 1 and counting up.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for DIP Components



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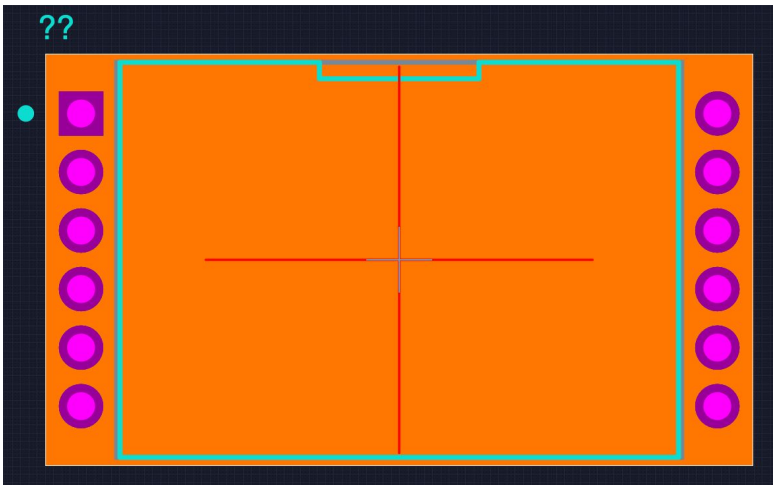
A dual in-line package (DIP) is an electronic component package with a rectangular housing and two parallel rows of electrical connecting pins. The package may be through-hole mounted to a printed circuit board or inserted in a socket.

Things to watch out for:

- Use a pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- If pin spacing allows, mark the polarity of the part by notching the end with pin one.
- The silkscreen should map the body of the part, which is inside the pins for most DIP parts (make sure not to put the silkscreen too close to the pins).
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for SDIP Components



A dual in-line package (DIP) is an electronic component package with a rectangular housing and two parallel rows of electrical connecting pins. The package may be through-hole mounted to a printed circuit board or inserted in a socket. The “S” stands for Shrink.

Things to watch out for:

- Use a pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- If pin spacing allows, mark the polarity of the part by notching the end with pin one.
- The silkscreen should map the body of the part, which is inside the pins for most DIP parts (make sure not to put the silkscreen too close to the pins).
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

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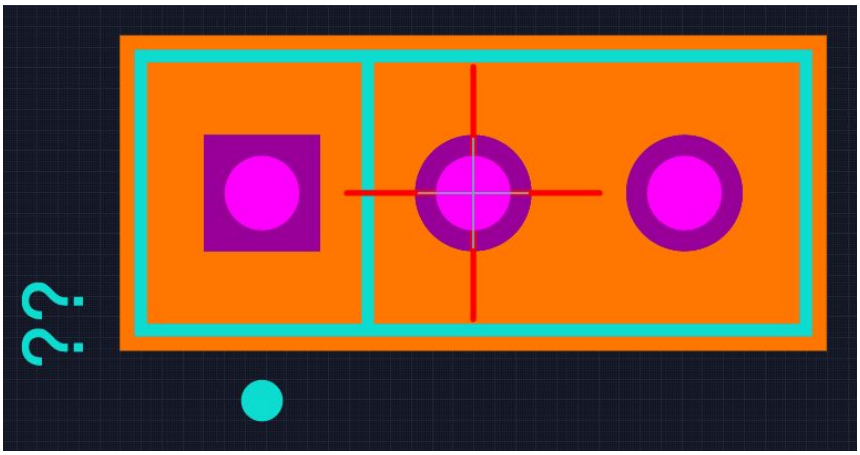
Specific Guidelines for SIP Components



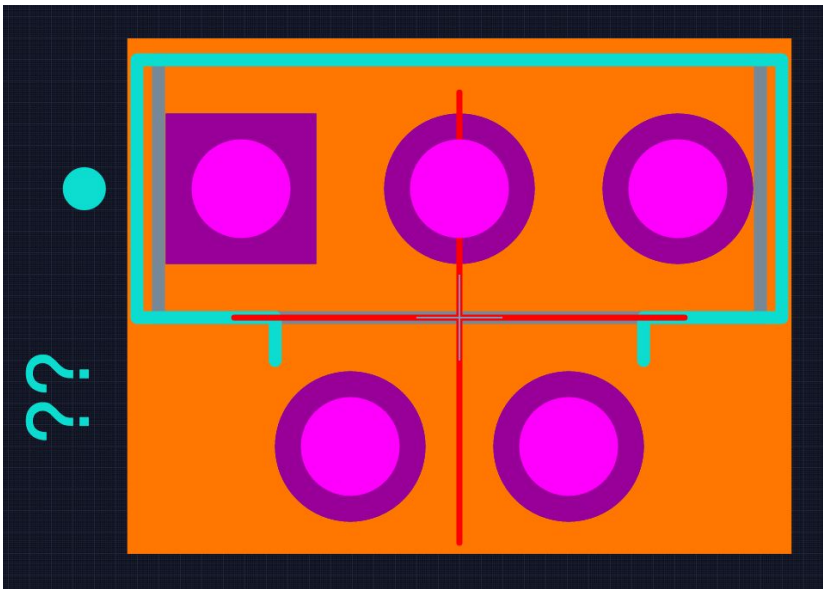
(rotated)

A single in-line (pin) package (SIP) has one row of connecting pins. It is not as popular as the DIP, but has been used for packaging RAM chips and multiple resistors with a common pin. SIPs group RAM chips together on a small board either by the DIP process or surface mounting SMD process. The board itself has a single row of pin-leads that resembles a comb extending from its bottom edge, which plug into a special socket on a system or system-expansion board.

Things to watch out for:

- Use a pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- If pitch allows (> 0.7mm), mark the polarity of the part by boxing pin one with silkscreen.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for ZIP Components



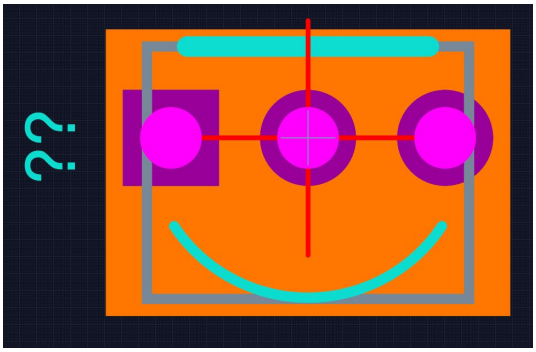
(rotated)

The zig-zag in-line package or ZIP was a short-lived packaging technology for integrated circuits, particularly dynamic RAM chips. It was intended as a replacement for dual in-line packaging (DIP). The package's pins protrude in two rows from one of the long edges. The two rows are staggered, giving them a zig-zag appearance, and allowing them to be spaced more closely than a rectangular grid would allow. The pins are inserted into holes in a printed circuit board, with the packages standing at right-angles to the board, allowing them to be placed closer together than DIPs of the same size.

Things to watch out for:

- Use a pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- The component outline (grey) should only mark the size of the body of the part and can overlap pads if that's where the body goes.
- The silkscreen should be as close to the outline as possible, without violating the minimum pad-to-silk clearance of 0.3mm
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.
- Add little silkscreen lines to indicate that the secondary row of pins is associated with the first row.

Specific Guidelines for TO92 Components



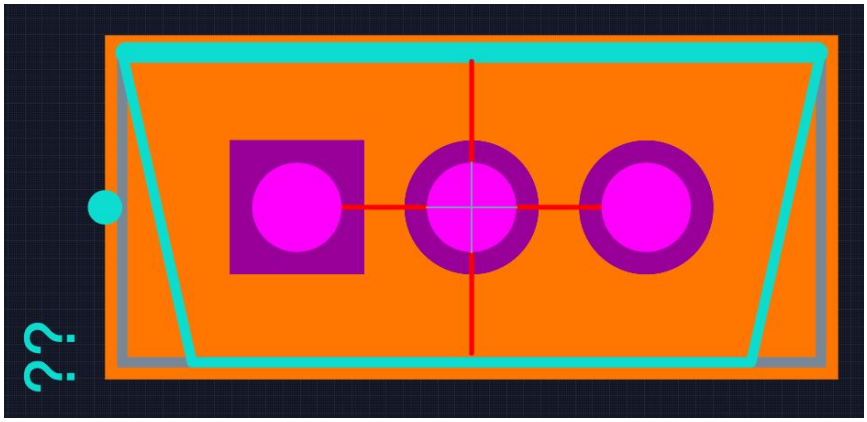
(rotated)

The TO-92 is a widely used style of semiconductor package mainly used for transistors. The case is often made of epoxy or plastic, and offers compact size at a very low cost.

Things to watch out for:

- No pin one silkscreen dot.
- The silkscreen should be semi-circular as shown in the picture above. Use the tool generator to achieve this semi-circular silkscreen.
- Unless specified differently in the datasheet, make the pin one pad square.
- Mark the polarity of the part with a thick (>0.3mm) silkscreen line.
- The component outline (grey) should only mark the size of the body of the part as a rectangle and can overlap pads if that's where the body goes.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.
- The silkscreen should be as close to the outline as possible, without violating the minimum pad-to-silk clearance of 0.3mm. It does not need to be a closed shape.
- Name the pins exactly as they are in the datasheet, if there are no names and the part is a transistor use EMITTER, BASE, COLLECTOR; if it's a mosfet use DRAIN, GATE, SOURCE; otherwise use numbers starting with 1 and counting up to 3.

Specific Guidelines for TO220 Components



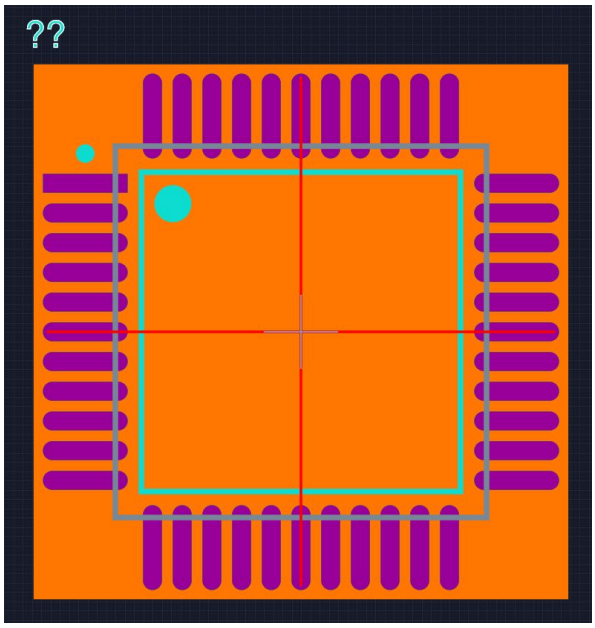
(rotated)

The TO-220 is a style of electronic component package, commonly used for discrete semiconductors as transistors and silicon-controlled rectifiers, as well as integrated circuits. The "TO" designation stands for "transistor outline". A notable characteristic is a metal tab with a hole, used in mounting the case to a heatsink. Components made in TO-220 packages can dissipate more heat than those constructed in TO-92 cases.

Things to watch out for:

- Use a pin one silkscreen dot.
- The silkscreen should be a trapezoid shape.
- Unless specified differently in the datasheet, make the pin one pad square.
- Mark the polarity of the part with a thick (>0.3mm) silkscreen line.
- The component outline (grey) should only mark the size of the body of the part as a rectangle shape and can overlap pads if that's where the body goes.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.
- The silkscreen should be as close to the outline as possible, without violating the minimum pad-to-silk clearance of 0.3mm. It does not need to be a closed shape.
- Name the pins exactly as they are in the datasheet, if there are no names and the part is a transistor use EMITTER, BASE, COLLECTOR; if it's a mosfet use DRAIN, GATE, SOURCE; otherwise use numbers starting with 1 and counting up to 3.

Specific Guidelines for QFP Components

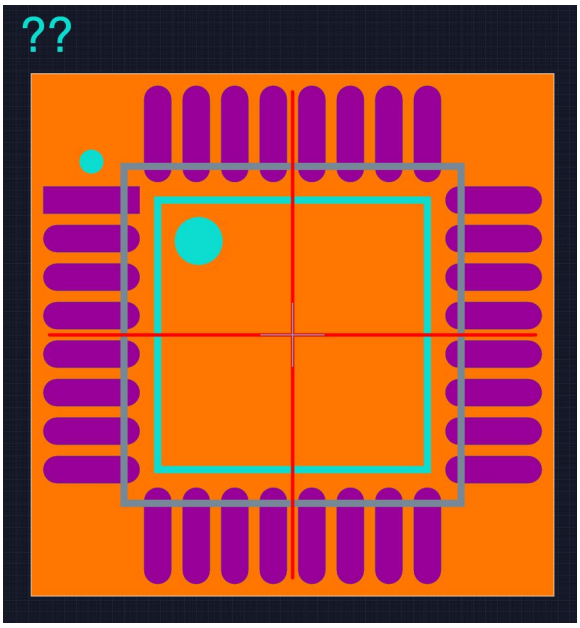


A QFP or Quad Flat Package is a surface mount integrated circuit package with "gull wing" leads extending from each of the four sides.

Things to watch out for:

- Use a pin one silkscreen dot.
- Place a second larger pin one silkscreen dot inside the component outline.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (which is inside the pins for most QFP parts), without violating the minimum pad-to-silk clearance of 0.3mm.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for TQFP Components

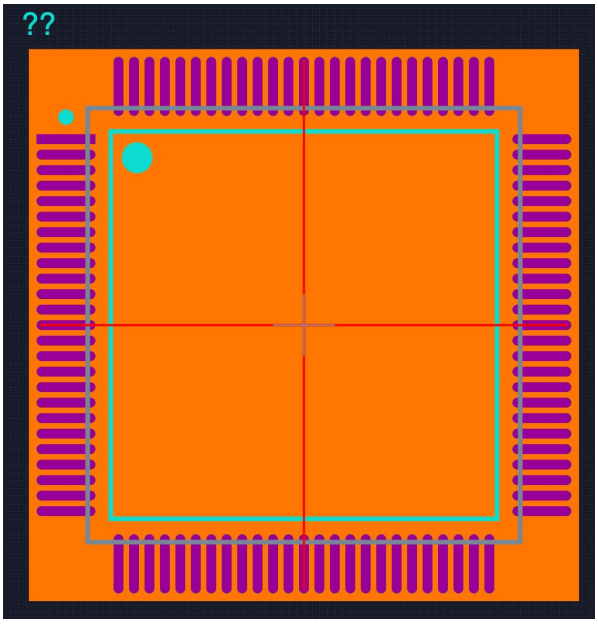


A QFP or Quad Flat Package is a surface mount integrated circuit package with "gull wing" leads extending from each of the four sides. The “T” stands for Thin.

Things to watch out for:

- Use a pin one silkscreen dot.
- Place a second larger pin one silkscreen dot inside the component outline.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (which is inside the pins for most QFP parts), without violating the minimum pad-to-silk clearance of 0.3mm.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for VQFP Components

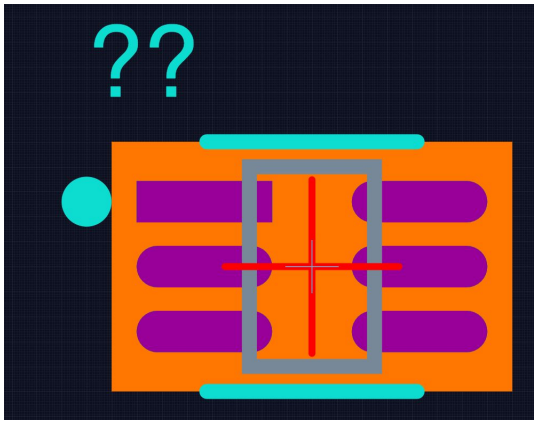


A QFP or Quad Flat Package is a surface mount integrated circuit package with "gull wing" leads extending from each of the four sides. The “V” stands for Very Small.

Things to watch out for:

- Use a pin one silkscreen dot.
- Place a second larger pin one silkscreen dot inside the component outline.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (which is inside the pins for most QFP parts), without violating the minimum pad-to-silk clearance of 0.3mm.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for PSOP Components



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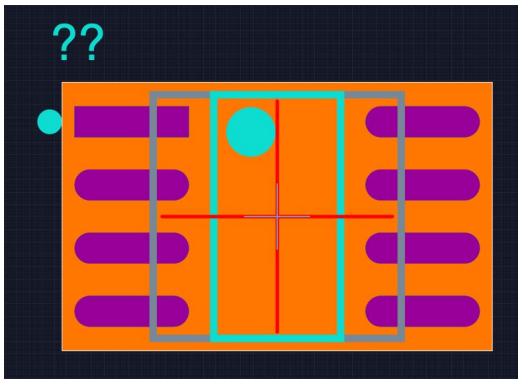
Plastic small-outline package (PSOP) is a surface mount package with a low profile and tightly packed leads.

Things to watch out for:

- Use a pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (which is above and below the pins for most PSOP parts). It does not need to be a closed shape, and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for SOIC Components

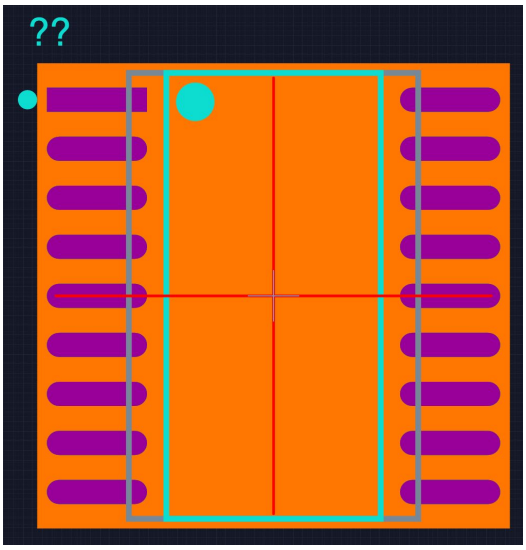


A Small Outline Integrated Circuit (SOIC) is a surface-mounted integrated circuit (IC) package which occupies an area about 30–50% less than an equivalent dual in-line package (DIP), with a typical thickness that is 70% less. They are generally available in the same pin-outs as their counterpart DIP ICs.

Things to watch out for:

- Use a pin one silkscreen dot.
- Space permitting, place a second larger pin one silkscreen dot inside the component outline.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (which is inside the pins for most SOIC parts). It does not need to be a closed shape, and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for SOIC (Wide) Components

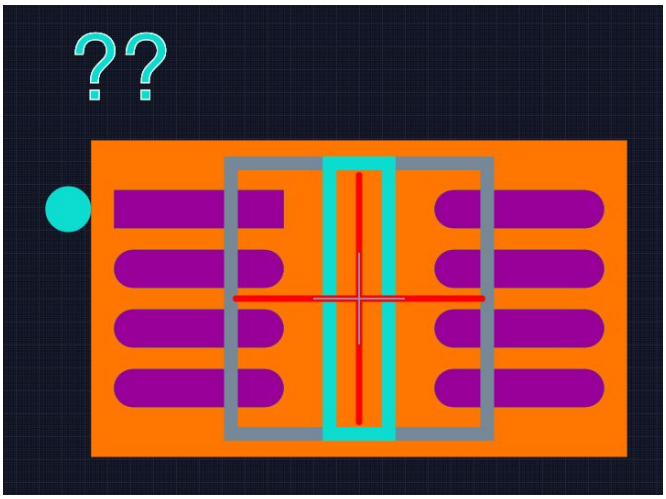


A Small Outline Integrated Circuit (SOIC) is a surface-mounted integrated circuit (IC) package which occupies an area about 30–50% less than an equivalent dual in-line package (DIP), with a typical thickness that is 70% less. They are generally available in the same pin-outs as their counterpart DIP ICs. The difference is mainly related to the parameters WB and WL.

Things to watch out for:

- Use a pin one silkscreen dot.
- Place a second larger pin one silkscreen dot inside the component outline.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (which is inside the pins for most SOIC parts), and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for SOIC (Mini) Components

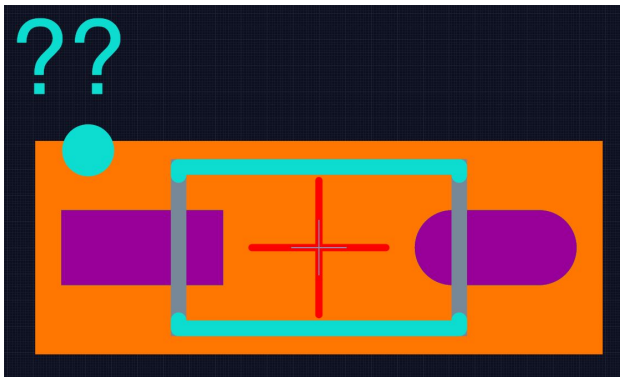


A Small Outline Integrated Circuit (SOIC) is a surface-mounted integrated circuit (IC) package which occupies an area about 30–50% less than an equivalent dual in-line package (DIP), with a typical thickness that is 70% less. They are generally available in the same pin-outs as their counterpart DIP ICs. The difference is mainly related to the parameters WB and WL.

Things to watch out for:

- Use a pin one silkscreen dot.
- Don't place a second larger pin one silkscreen dot inside the component outline, as there won't be enough space.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (which is inside the pins for most SOIC parts, but may need to be just top and bottom lines). It does not need to be a closed shape, and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for SOD123 Components



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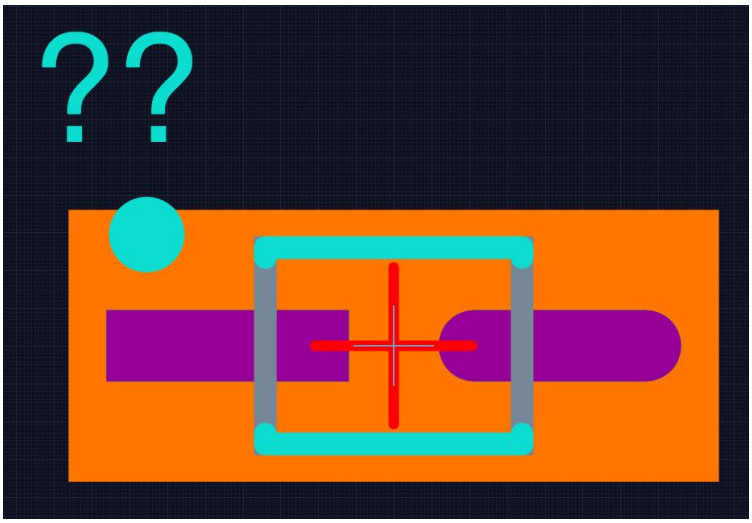
Small Outline Diode (SOD) is a designation for a group of semiconductor packages for surface mounted diodes. The standard includes several variants such as SOD-123, SOD-323, SOD-523 and SOD-923. SOD-123 is the largest, SOD-923 is the smallest.

Things to watch out for:

- Use a pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (a rectangle with cutouts for the pins). It does not need to be a closed shape, and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- Name the pins exactly as they are in the datasheet, if there are no names and the part has polarity use CATHODE (PIN 1) and ANODE (PIN 2), otherwise use 1 & 2.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for SOD323 Components



Small Outline Diode (SOD) is a designation for a group of semiconductor packages for surface mounted diodes. The standard includes several variants such as SOD-123, SOD-323, SOD-523 and SOD-923. SOD-123 is the largest, SOD-923 is the smallest.

Things to watch out for:

- Use a pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (a rectangle with cutouts for the pins). It does not need to be a closed shape, and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- Name the pins exactly as they are in the datasheet, if there are no names and the part has polarity use CATHODE (PIN 1) and ANODE (PIN 2), otherwise use 1 & 2.

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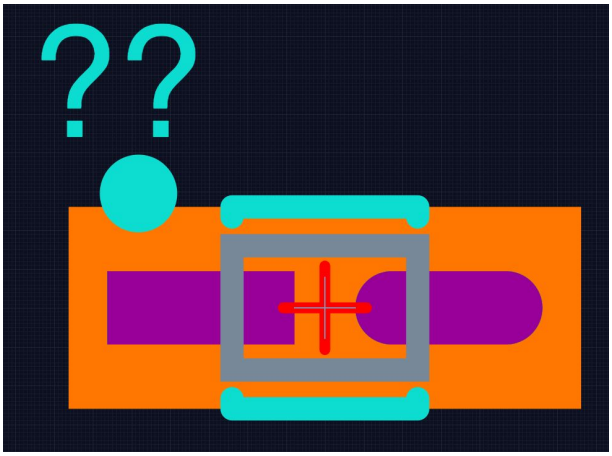
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for SOD523 Components

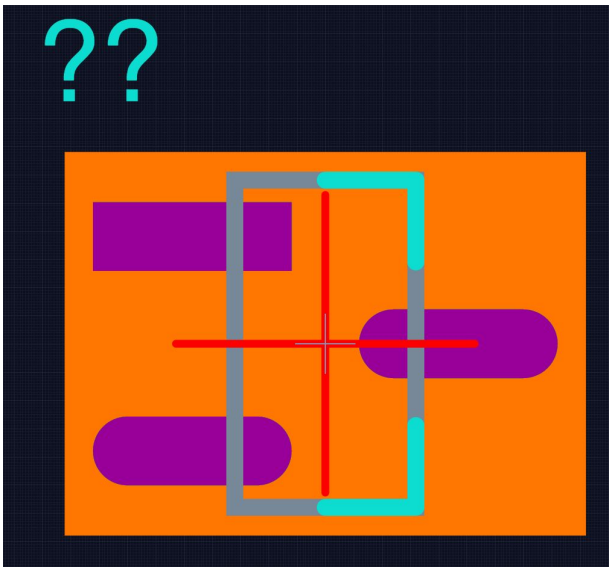


Small Outline Diode (SOD) is a designation for a group of semiconductor packages for surface mounted diodes. The standard includes several variants such as SOD-123, SOD-323, SOD-523 and SOD-923. SOD-123 is the largest, SOD-923 is the smallest.

Things to watch out for:

- Use a pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (a rectangle with cutouts for the pins). It does not need to be a closed shape, and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- Name the pins exactly as they are in the datasheet, if there are no names and the part has polarity use CATHODE (PIN 1) and ANODE (PIN 2), otherwise use 1 & 2.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for SOT23 Components

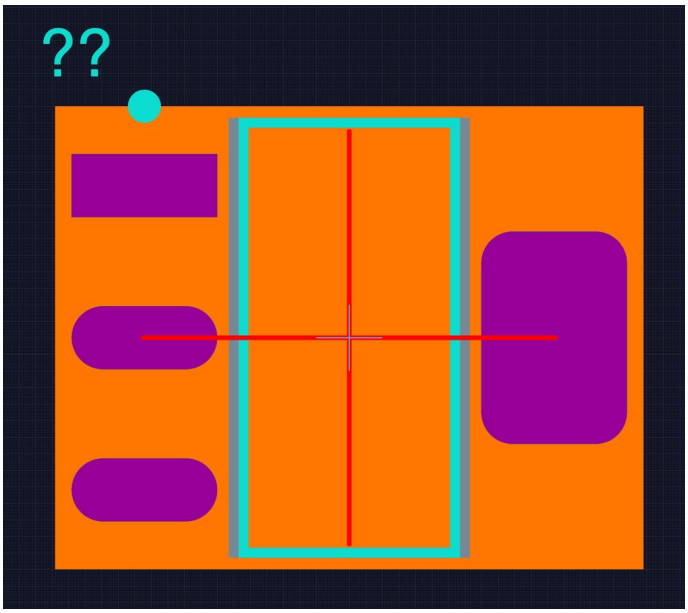


A small outline transistor (SOT) is a small footprint, discrete surface mount transistor commonly used in consumer electronics.

Things to watch out for:

- Don’t use a pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (two corners with cutouts for the pins). It does not need to be a closed shape, and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- Name the pins exactly as they are in the datasheet, if there are no names and the part is a transistor use EMITTER, BASE, COLLECTOR; if it’s a mosfet use DRAIN, GATE, SOURCE; otherwise use numbers starting with 1 and counting up to 3.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for SOT223 Components

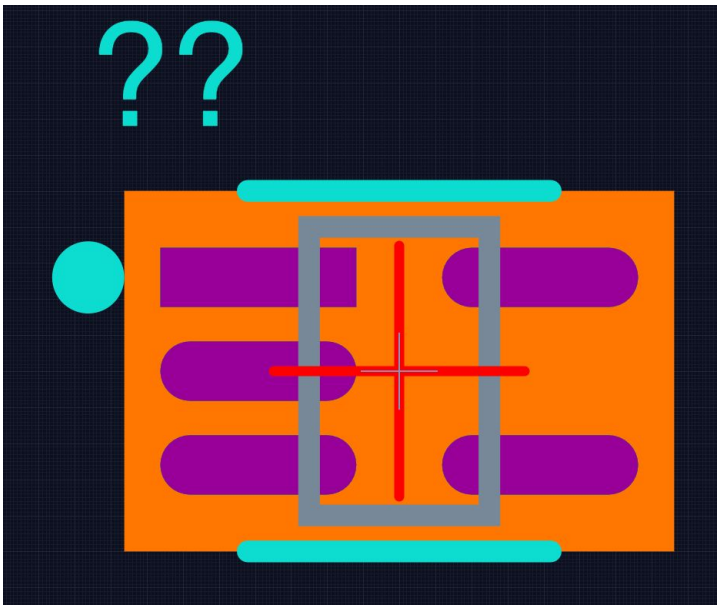


A small outline transistor (SOT) is a small footprint, discrete surface mount transistor commonly used in consumer electronics.

Things to watch out for:

- Use a pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (a rectangle inside the pins), and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- Name the pins exactly as they are in the datasheet, if there are no names and the part is a transistor use EMITTER, BASE, COLLECTOR; if it's a mosfet use DRAIN, GATE, SOURCE; otherwise use numbers starting with 1 and counting up to 3.
- Name any unused pins exactly as they are in the datasheet, if there are no names then use NC (stands for no connect).
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for SOT3x3 Components

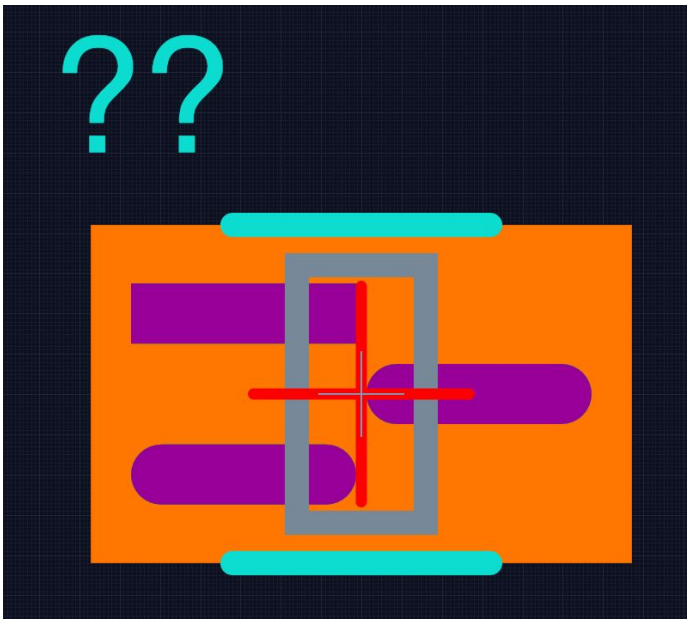


A small outline transistor (SOT) is a small footprint, discrete surface mount transistor commonly used in consumer electronics.

Things to watch out for:

- Use a pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (top and bottom lines). It does not need to be a closed shape, and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- Name the pins exactly as they are in the datasheet, if there are no names and the part is a transistor use EMITTER, BASE, COLLECTOR; if it's a mosfet use DRAIN, GATE, SOURCE; otherwise use numbers starting with 1 and counting up to 3.
- Name any unused pins exactly as they are in the datasheet, if there are no names then use NC (stands for no connect).
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for SOT523 Components

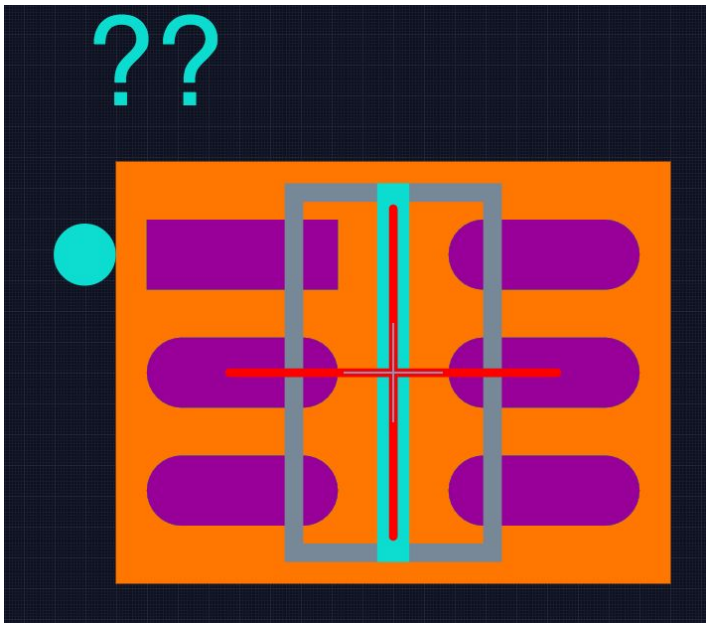


A small outline transistor (SOT) is a small footprint, discrete surface mount transistor commonly used in consumer electronics.

Things to watch out for:

- Don’t use a pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (top and bottom lines). It does not need to be a closed shape, and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- Name the pins exactly as they are in the datasheet, if there are no names and the part is a transistor use EMITTER, BASE, COLLECTOR; if it’s a mosfet use DRAIN, GATE, SOURCE; otherwise use numbers starting with 1 and counting up to 3.
- Name any unused pins exactly as they are in the datasheet, if there are no names then use NC (stands for no connect).
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for TSOT Components

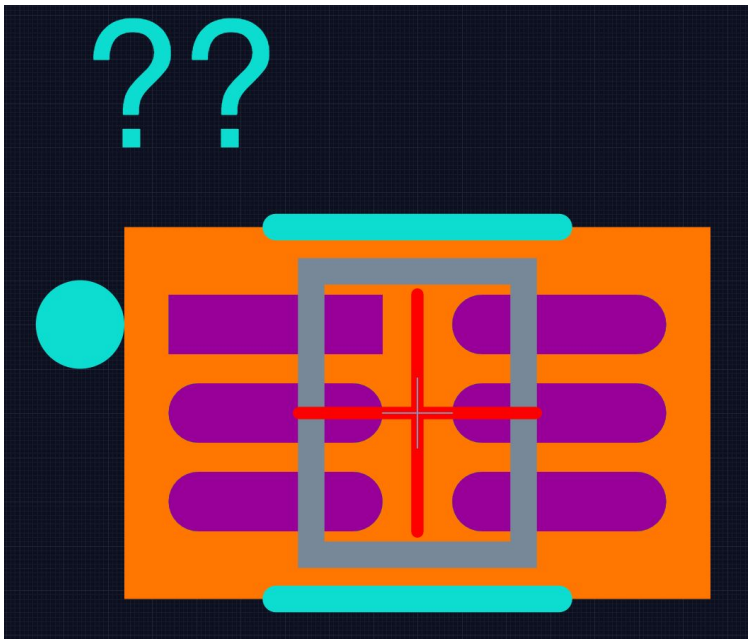


A small outline transistor (SOT) is a small footprint, discrete surface mount transistor commonly used in consumer electronics.

Things to watch out for:

- Use a pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (thick central line, or top and bottom lines). It does not need to be a closed shape, and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- Name the pins exactly as they are in the datasheet, if there are no names and the part is a transistor use EMITTER, BASE, COLLECTOR; if it's a mosfet use DRAIN, GATE, SOURCE; otherwise use numbers starting with 1 and counting up to 3.
- Name any unused pins exactly as they are in the datasheet, if there are no names then use NC (stands for no connect).
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for SOT563 Components

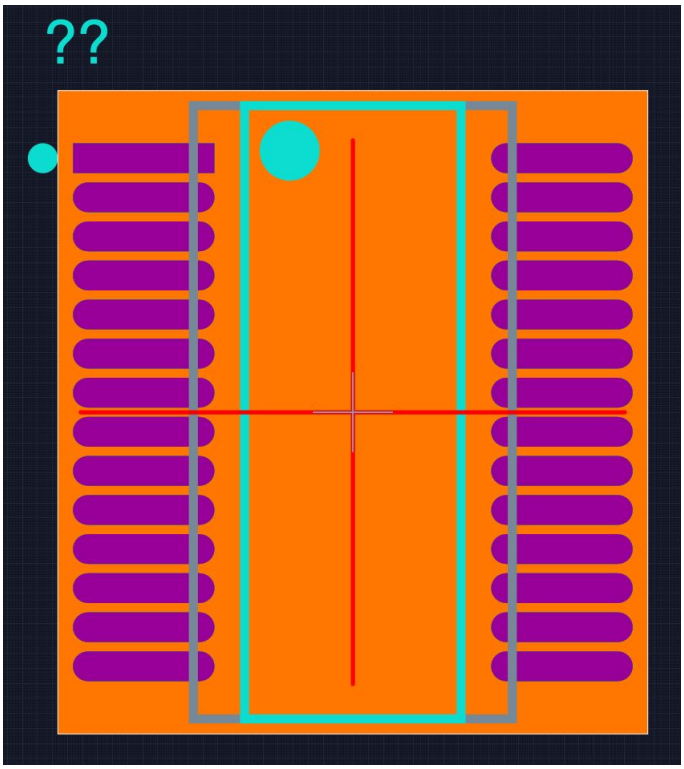


A small outline transistor (SOT) is a small footprint, discrete surface mount transistor commonly used in consumer electronics.

Things to watch out for:

- Use a pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (top and bottom lines). It does not need to be a closed shape, and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for SSOP Components

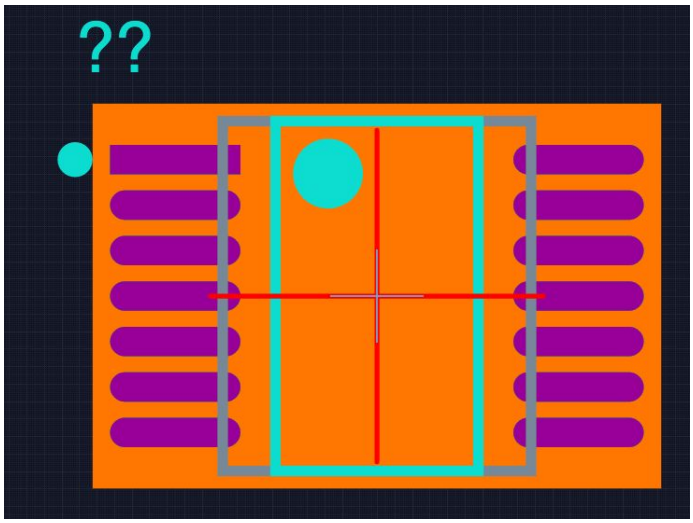


Shrink small outline package (SSOP) chips have "gull wing" leads protruding from the two long sides. The body size of a SOP was compressed and the lead pitch tightened to obtain a smaller version SOP. This yields an IC package which is a significant reduction in the size (compared to standard package).

Things to watch out for:

- Use a pin one silkscreen dot.
- Place a second larger pin one silkscreen dot inside the component outline.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (which is inside the pins for most SSOP parts), and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for TSSOP Components

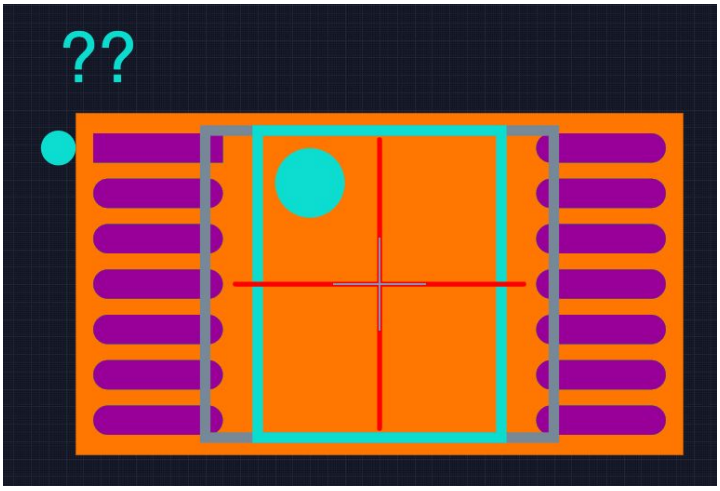


A TSSOP (thin-shrink small outline package) is a rectangular, thin body size component. A Type I TSSOP has legs protruding from the width portion of the package.

Things to watch out for:

- Use a pin one silkscreen dot.
- Place a second larger pin one silkscreen dot inside the component outline.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (which is inside the pins for most TSSOP parts), and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for TSSOP2 Components



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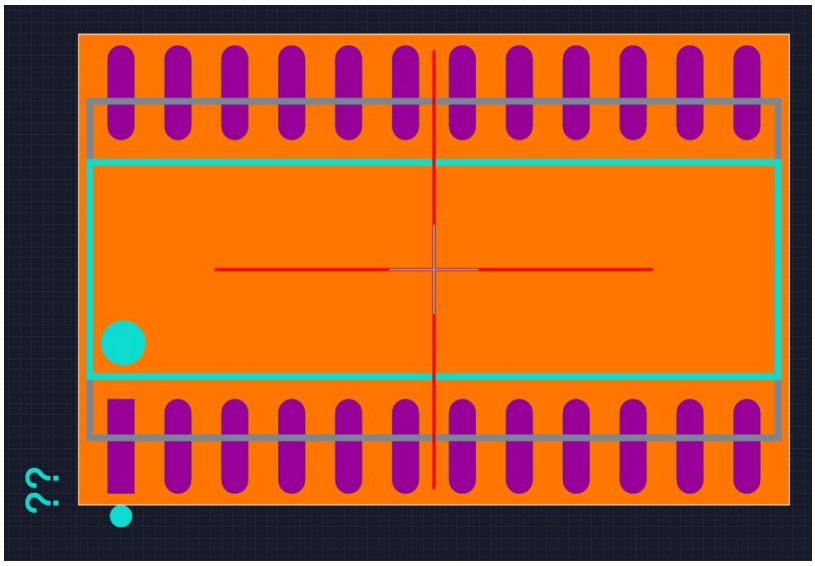
A TSSOP (thin-shrink small outline package) is a rectangular, thin body size component. A Type II TSSOP has the legs protruding from the length portion of the package.

Things to watch out for:

- Use a pin one silkscreen dot.
- Place a second larger pin one silkscreen dot inside the component outline.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (which is inside the pins for most TSSOP2 parts), and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for SOJ Components



(rotated)

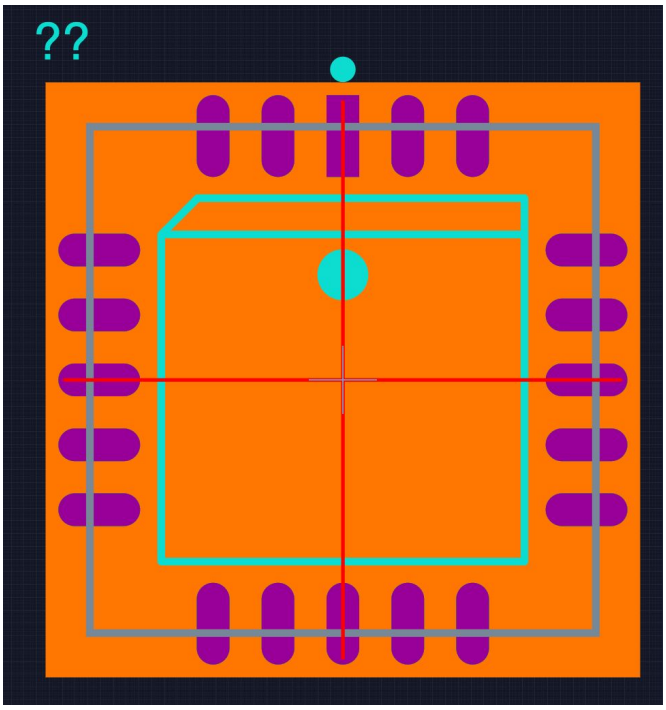
Small outline J-leaded package (SOJ) is a version of SOIC with J-type leads instead of gull-wing leads.

Things to watch out for:

- Use a pin one silkscreen dot.
- Place a second larger pin one silkscreen dot inside the component outline.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (which is inside the pins for most SOJ parts), and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

For more information or component creation services visit EEConcierge.com

Specific Guidelines for PLCC Components

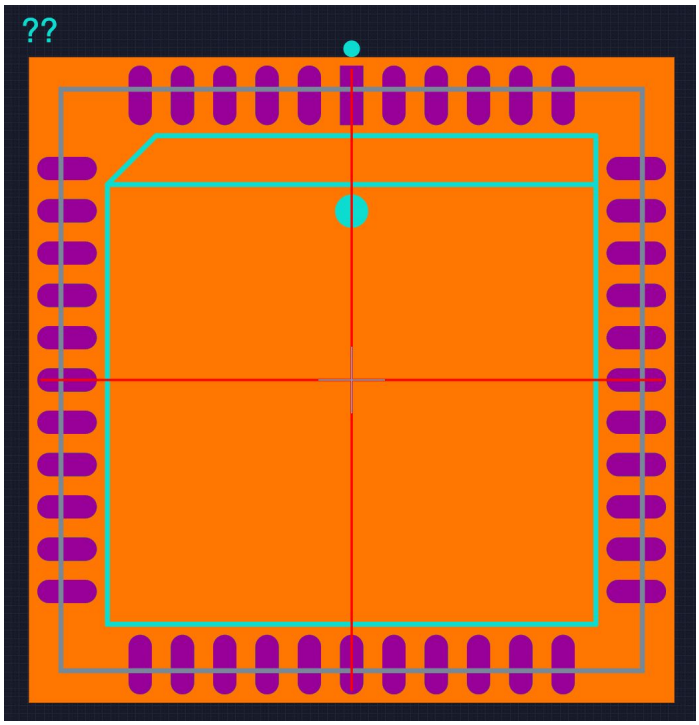


A plastic leaded chip carrier (PLCC) has a rectangular plastic housing. It is a reduced cost evolution of the ceramic leadless chip carrier (CLCC).

Things to watch out for:

- Use a pin one silkscreen dot.
- Place a second larger pin one silkscreen dot inside the component outline, below pin one.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (which is inside the pins for most PLCC parts), and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- The silkscreen should be angled in the corner, like the part is.
- The silkscreen should also have a second line at the top to mark polarity.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for JLCC Components

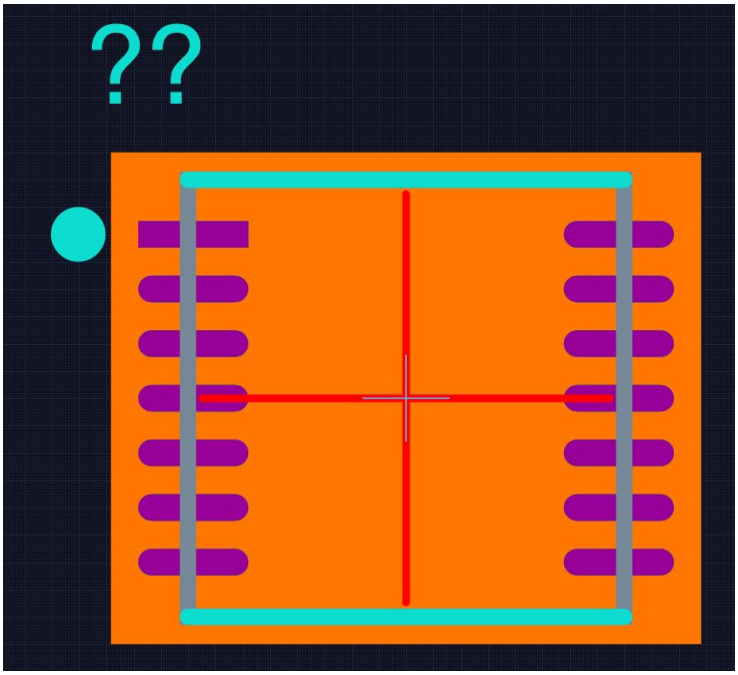


J-Leaded Ceramic or Metal Chip Carrier.

Things to watch out for:

- Use a pin one silkscreen dot.
- Place a second larger pin one silkscreen dot inside the component outline, below pin one.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (which is inside the pins for most PLCC parts), and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- The silkscreen should be angled in the corner, like the part is.
- The silkscreen should also have a second line at the top to mark polarity.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for DFN Components

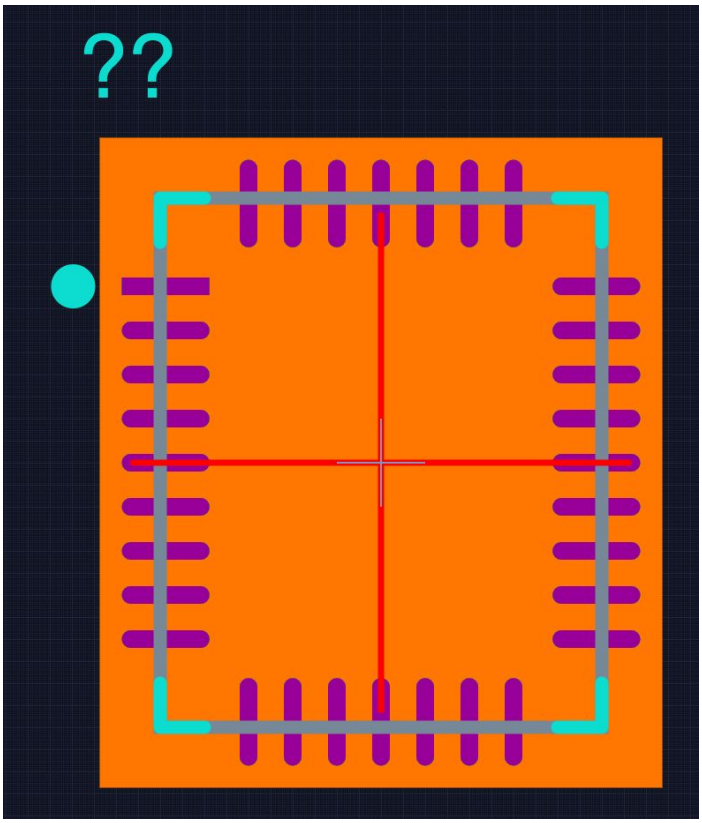


Flat no-leads packages such as dual flat no-lead package (DFN) is a near chip scale plastic encapsulated package made with a planar copper lead frame substrate. Perimeter lands on the package bottom provide electrical connections to the PCB. Flat no-lead packages include an exposed thermal pad to improve heat transfer out of the IC (into the PCB).

Things to watch out for:

- Use a pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (top and bottom lines). It does not need to be a closed shape, and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for QFN Components

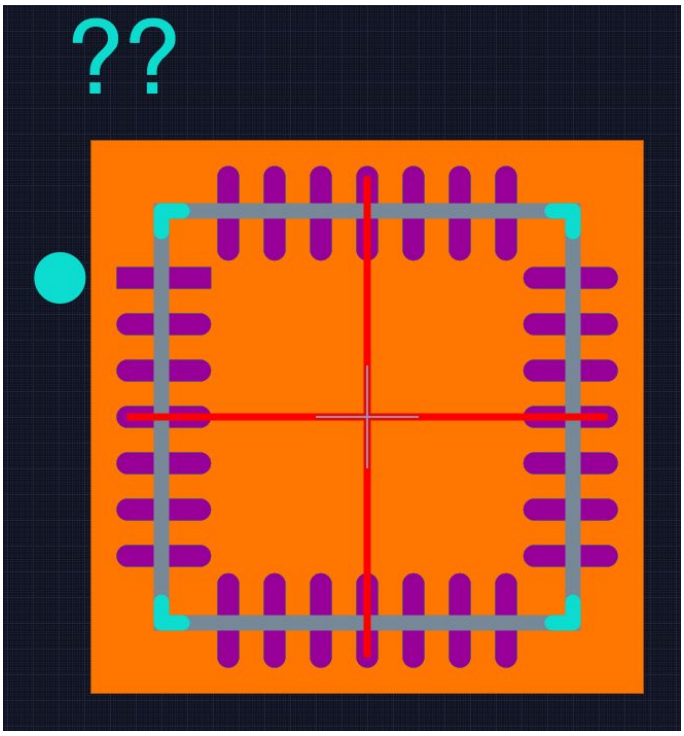


Flat no-leads packages such as quad-flat no-leads (QFN) is a near chip scale plastic encapsulated package made with a planar copper lead frame substrate. Perimeter lands on the package bottom provide electrical connections to the PCB. Flat no-lead packages include an exposed thermal pad to improve heat transfer out of the IC (into the PCB). The QFN package is similar to the quad-flat package, and a ball grid array.

Things to watch out for:

- Use a pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (corners in each corner with cutouts for the pins). It does not need to be a closed shape, and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for TQFN Components

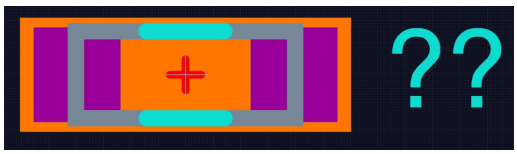


Flat no-leads packages such as quad-flat no-leads (QFN) is a near chip scale plastic encapsulated package made with a planar copper lead frame substrate. Perimeter lands on the package bottom provide electrical connections to the PCB. Flat no-lead packages include an exposed thermal pad to improve heat transfer out of the IC (into the PCB). The “T” stands for Thin.

Things to watch out for:

- Use a pin one silkscreen dot.
- Unless specified differently in the datasheet, make the pin one pad square.
- The silkscreen should be as close to the outline as possible (corners in each corner with cutouts for the pins). It does not need to be a closed shape, and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for Chip Resistor Components



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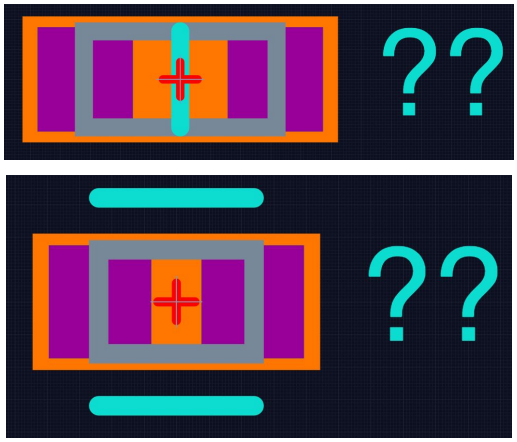
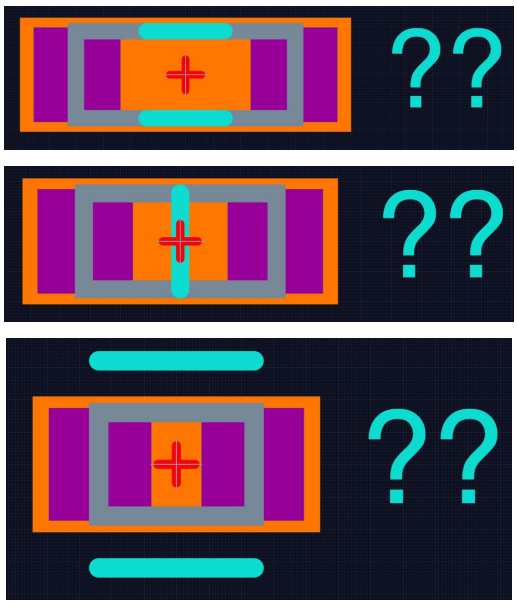


The surface mount version of the resistor.

Things to watch out for:

- Don't use a pin one silkscreen dot.
- The silkscreen should be as close to the outline as possible (in descending order: a rectangle with the left and right cut off for the pins, a vertical line in the center of the part, lines outside the part marking and top and bottom). It does not need to be a closed shape, and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- Name the pins 1 & 2
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for Chip Capacitor Components



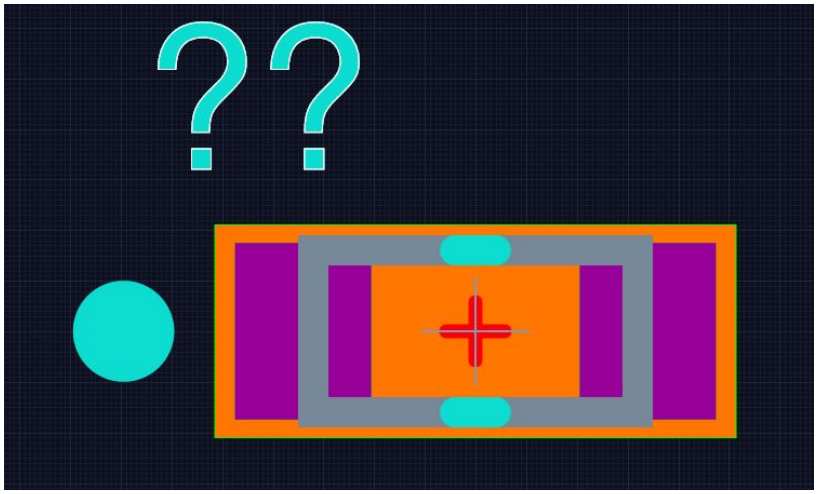
The surface mount version of the capacitor.

For more information or component creation services visit EEConcierge.com

Things to watch out for:

- Use a pin one silkscreen dot if the part has polarity.
- The silkscreen should be as close to the outline as possible (in descending order: a rectangle with the left and right cut off for the pins, a vertical line in the center of the part, lines outside the part marking and top and bottom). It does not need to be a closed shape, and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- Name the pins CATHODE (PIN 1) and ANODE (PIN 2) if the part has polarity, otherwise 1 & 2.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for LED Components



A light-emitting diode (LED) is a two-lead semiconductor light source. It is a p–n junction diode, which emits light when activated. When a suitable voltage is applied to the leads, electrons are able to recombine with electron holes within the device, releasing energy in the form of photons.

Things to watch out for:

- Use a pin one silkscreen dot.
- The silkscreen should be as close to the outline as possible (in descending order: a rectangle with the left and right cut off for the pins, a vertical line in the center of the part, lines outside the part marking and top and bottom). It does not need to be a closed shape, and be careful not to violate the minimum pad-to-silk clearance of 0.3mm.
- Name the pins CATHODE (PIN 1) and ANODE (PIN 2) if there are two.
- Name the pins COLOR_CATHODE and COLOR_ANODE if there are multiple colors. For example GREEN_CATHODE, GREEN_ANODE, RED_CATHODE and RED_ANODE for a 4 pin red & green LED.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

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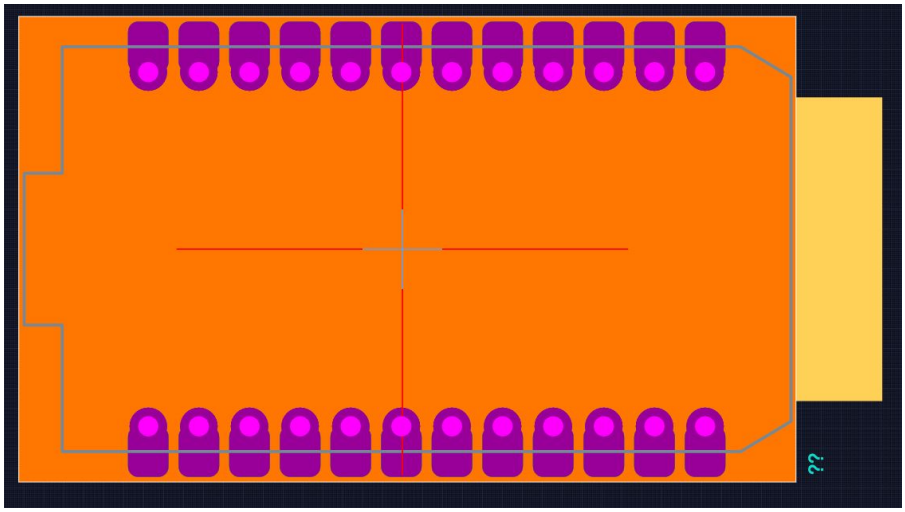
Specific Guidelines for Non-IPC Components



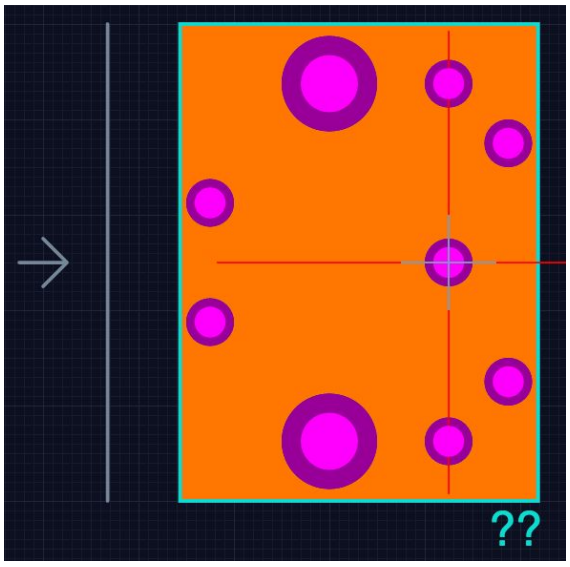
(rotated)

These are the guidelines for non-connector components that don't fall into any of the above IPC standard packages.

Things to watch out for:

- Try to use a generator that's close to the desired footprint and if necessary tweak it once generated.
- Review the Common Mistakes Made section.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.

Specific Guidelines for Non-IPC Connectors



For more information or component creation services visit EEConcierge.com

These are the guidelines for connector components that don't fall into any of the above IPC standard packages.

Things to watch out for:

- Try to use a generator that's close to the desired footprint and if necessary tweak it once generated.
- Review the Common Mistakes Made section.
- The placement courtyard (orange) should extend 0.1mm beyond the maximum of the pads or maximum dimensions of the component body.